FIRST DRAFT

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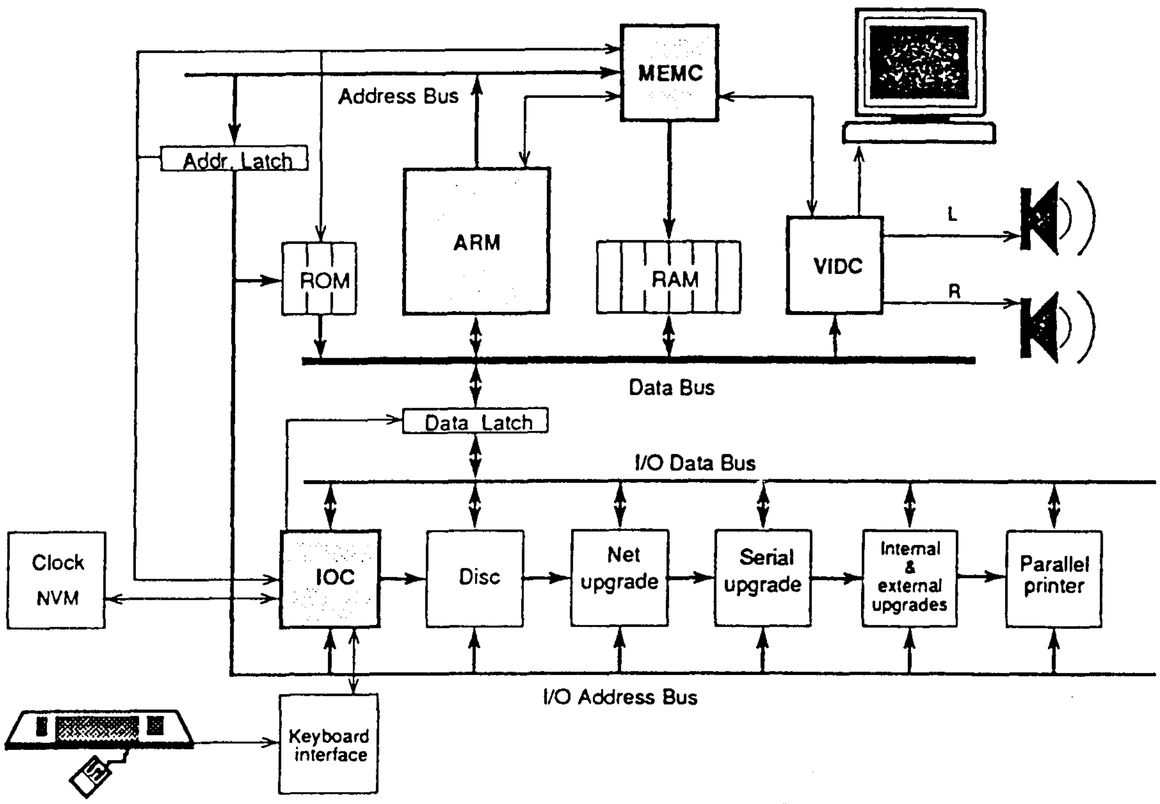
Contents

System Description

Introduction

The A3000 computer is built around the ARM chip set, comprising the Acorn Risc Machine (ARM) itself, the Memory Controller (MEMC), Video Controller (VIDC) and Input Output Controller (IOC).

A block diagram of the A3000 is shown below:



General

The ARM (Acorn Risc Machine) IC is a pipelined, 32-bit reduced instruction set microprocessor which accepts instructions and manipulates data via a high speed 32-bit data bus and 26-bit address bus giving a 64 Mbyte uniform address space. The ARM supports virtual memory systems using a simple but powerful instruction set with good high-level language compiler support.

The Memory Controller (MEMC) acts as the interface between the ARM, the Video Controller, I/O Controllers, Read-Only Memory (ROM) and Dynamic memory devices (DRAM), providing all the critical system timing signals including processor clocks.

1 or 2 Mbyte of DRAM is connected to MEMC which provides all signals and refresh operations. A Logical to Physical Translator maps the Physical Memory into a 32 Mbyte Logical address space (with three levels of protection) allowing Virtual Memory and Multi-Tasking operations to be implemented. Fast page mode DRAM accesses are used to maximise memory bandwidth. The VIDC requests data from the RAM when required and buffers it in one of three FIFOs before using it. Data is requested in blocks of four 32-bit words, allowing efficient use of paged-mode DRAM without locking the system data bus for long periods.

MEMC supports Direct Memory Access (DMA) operations with a set of programmable DMA Address Generators which provide a circular buffer for Video data, a linear buffer for Cursor data and a double buffer for Sound data.

The Input Output Controller (IOC) controls the I/O bus, expansion cards and provides basic functions such as the keyboard interface, system timers, interrupt masks and control registers. It supports a number of different peripheral cycles and all I/O accesses are memory mapped.

The Video Controller (VIDC) takes video data from memory under DMA control, serialises it and passes it through a colour look-up palette and converts it to analogue signals for driving the CRT guns. VIDC also controls all the display timing parameters and controls the position and pattern of the cursor sprite. In addition, it incorporates an exponential Digital to Analogue Converter (DAC) and stereo image table for the generation of high quality sound from data in the DRAM.

VIDC is a highly programmable device, offering a very wide choice of display formats. The colour look-up palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colours or an external video source.

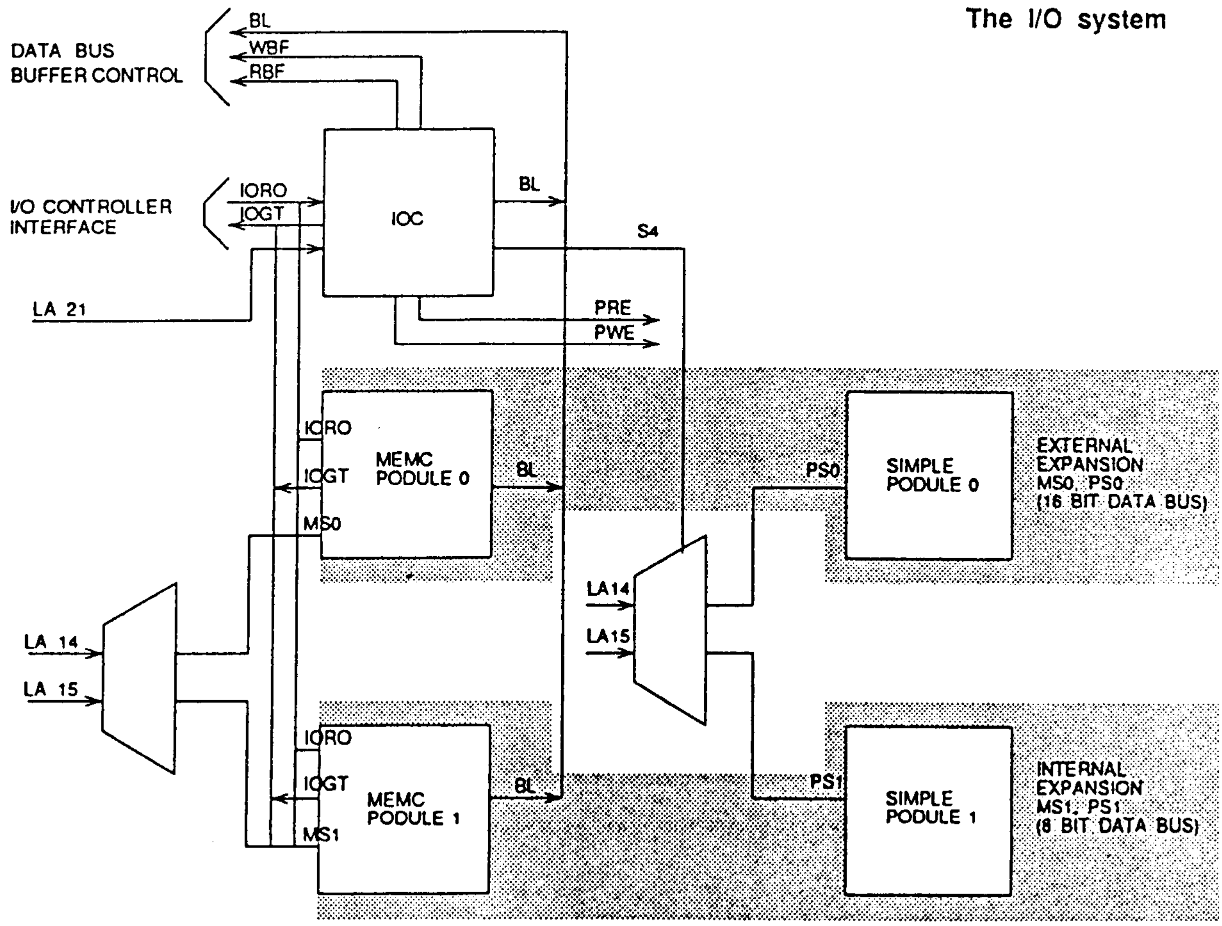
The cursor sprite is 32 pixels wide and any number of rasters high. Three simultaneous colours (again from a choice of 4096) are supported and any pixel can be defined as transparent, making possible cursors of many shapes. It can be positioned anywhere on the screen. The sound system implemented on the device can support up to 8 channels, each with a separate stereo position.

The I/O system

The I/O system is controlled by the I/O Controller IOC and the Memory Controller MEMC. The I/O Bus supports all the internal peripherals and the expansion cards. Details of the expansion bus can be found elsewhere in this manual.

This section is intended to give the reader a general understanding of the A3000 I/O system and should not be used to program the I/O system directly. The implementation details are liable to change at any time and only the published software interfaces should be used to manipulate the I/O system. Future systems may have a different implementation of the I/O system, and in particular the addresses (and number) of expansion card locations may move. For this reason, and to ensure that any device may be plugged into any slot, all driver code for expansion cards must be relocatable. References to the direct expansion card addresses should never be used. It is up to the machine operating system, in conjunction with the expansion card ID, to determine the address at which an expansion card should be accessed. To this extent, some of the following sections are for background information only.

The I/O system



System Architecture

The I/O system (which includes expansion card devices) consists of a 16-bit data bus (BD[0:15]) a buffered address bus (LA[2:21]) and various control and timing signals. The I/O data bus is independent of the main 32-bit system data bus, being separated from it by bidirectional latches and buffers. In this way the I/O data bus can run at much slower speeds than the main system bus to cater for slower peripheral devices. The latches between the two buses, and hence the I/O bus timing are controlled by the I/O controller, IOC. The IOC caters for 4 different cycle speeds (slow, medium, fast and synchronous).

A typical A3000 I/O system is shown in the diagram below. For clarity, the data and address buses are omitted from this diagram.

System memory map

The system memory map is defined by the MEMC, and is shown below. Note that all system components, including I/O devices, are memory mapped.

I/O space memory map

This IOC-controlled space has allocation for simple expansion cards and MEMC expansion cards.

Data bus mapping

The I/O data bus is 16 bits wide (8 bits wide for internal expansion cards). Bytewide accesses are used for 8-bit peripherals. The I/O data bus (BD[0:15]) connects to the main system data bus (D[0:31]) via a set of bidirectional data latches.

The mapping of the BD[0:15] bus onto the D[0:31] bus is as follows:

During a WRITE (ie ARM to peripheral) BD[0:15] is mapped to D[16:31].

During a READ (ie peripheral to ARM) BD[0:15] is mapped to D[0:15].

Byte accesses

To access bytewide expansion cards, byte instructions are used. A byte store instruction will place the written byte on all four bytes of the word, and will therefore correctly place the desired value on the lowest byte of the I/O bus. A byte or word load may be used to read a bytewide expansion card into the lowest byte of an ARM register.

Half-word accesses

To access a 16-bit wide expansion card, half-word instructions are used. When storing, the half-word is placed on the upper 16 bits, D[16:31]. To maintain upwards compatibility with future machines, half-word stores replicate the written data on the lower half-word, D[0:15]. When reading, the upper 16 bits are undefined.

Expansion card identification

It is important that the system is able to identify what expansion cards (if any) are present, and where they are. This is done by reading the Podule (expansion card) Identification (PI) byte, or bytes, from the Podule Identification Field.

System memory map

Read	Write	Hex address
		3FFFFFF
ROM (high)	Logical to Physical address translator	
		3800000
ROM (low)	DMA address generators	
		3600000
ROM (low)	Video Controller	
		3400000
Input/Output Controllers	Input/Output Controllers	
		3000000
Physically mapped RAM	Physically mapped RAM	
		2000000
Logically mapped RAM	Logically mapped RAM	
		0000000

I/O address memory mapping

All I/O accesses are memory mapped. IOC is connected as detailed in this table:

IOC	ARM
OE	LA[21]
T[1]	LA[20]
T[0]	LA[19]
B[2]	LA[18]
B[1]	LA[17]
B[0]	LA[16]

Internal Register Memory Map

Address	Read	Write
3200000H	Control	Control
3200004H	Serial Rx Data	Serial Tx Data
3200008H	-	-
320000CH	-	-
3200010H	IRQ status A	-
3200014H	IRQ request A	IRQ clear
3200018H	IRQ mask A	IRQ mask A
320001CH	-	-
3200020H	IRQ status B	-
3200024H	IRQ request B	-
3200028H	IRQ mask B	IRQ mask B
320002CH	-	-
3200030H	FIQ status	-
3200034H	FIQ request	-
3200038H	FIQ mask	FIQ mask
320003CH	-	-
3200040H	T0 count Low	T0 latch Low
3200044H	T0 count High	T0 latch High
3200048H	-	T0 go command
320004CH	-	T0 latch command
3200050H	T1 count Low	T1 latch Low
3200054H	T1 count High	T1 latch High
3200058H	-	T1 go command
320005CH	-	T1 latch command
3200060H	T2 count Low	T2 latch Low
3200064H	T2 count High	T2 latch High
3200068H	-	T2 go command
320006CH	-	T2 latch command
3200070H	T3 count Low	T3 latch Low
3200074H	T3 count High	T3 latch High
3200078H	-	T3 go command
320007CH	-	T3 latch command

Peripheral address

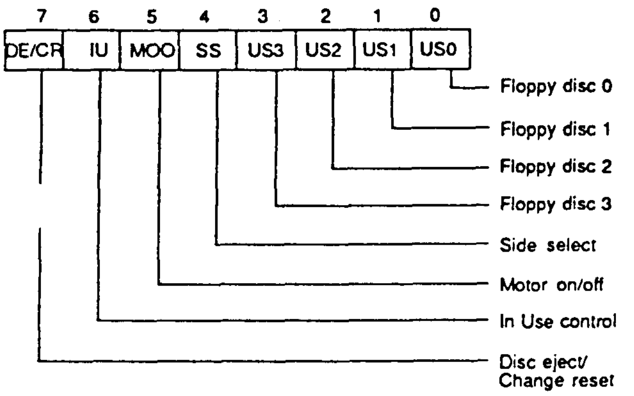
Cycle Type	Bk	Base Address	IC	Use
Fast	1	&3310000	1772	Floppy disc controller
Sync	2	&33A0000	6854	Econet controller*
Sync	3	&33B0000	6551	Serial line controller*
Med.	5	&32D0000	HD63463	Hard disc**
Med.	5	&32D0020	HD63463	Hard disc**
Med.	5	&32D0008	HD63463	Hard disc**
Med.	5	&32D0028	HD63463	Hard disc**
Fast	5	&3350010	HC374	Printer Data
Fast	5	&3350018	HC574	Latch B
Fast	5	&3350040	HC574	Latch A
	6	-	-	Reserved
Slow	4	&3244000	Podule	Internal expansion
Med.	4	&32C4000	Podule	Internal expansion
Fast	4	&3344000	Podule	Internal expansion
Sync	4	&33C4000	Podule	Internal expansion
Slow	4	&3240000	Podule	External expansion
Med.	4	&32C0000	Podule	External expansion
Fast	4	&3340000	Podule	External expansion
Sync		&33C0000	Podule	External expansion
Slow	7	&3270000	Podule	Extended ext expansion

*if fitted
** not fitted

I/O Programming Details

External latch A

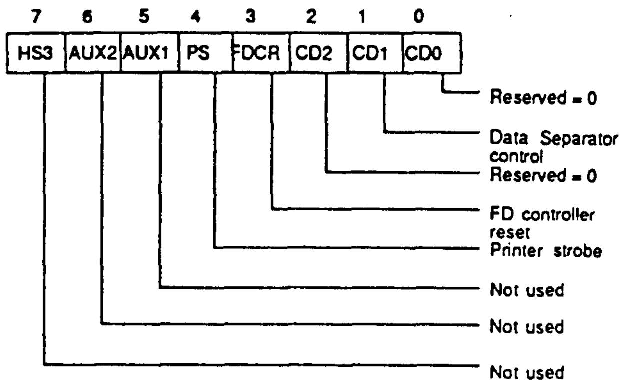
External Latch A is a write only latch used to control parts of the floppy disc sub-system:



Bit	Name	Function
0-3	Floppy disc sel.	These bits select the floppy disc drive 0 through 3 when written LOW. Only one bit should be LOW at any one time.
4	Side select	This controls the side select line of the floppy disc interface. 0 = Side 1 (upper) 1 = Side 0 (lower)
	Floppy motor	This bit control the floppy disc on/off control motor line. Its exact use depends on the type of drive.
6	In Use	This bit controls the IN USE line of the floppy disc. Its exact use depends on the type of drive.
7		Not used.

External latch B

The External Latch B is a write only register shared between several users who must maintain a consistent RAM copy. Updates must be made with IRQ disabled.



Bit	Name	Function
0-2		CD[0:2] should be programmed CD[0.2] LOW for future compatibility. CD[1] controls the floppy disc data separator format. CD[1] = 0 Double Density CD[1] = 1Single Density
Bit 3	FDCR	This controls the floppy disc controller reset line. When programmed LOW, the controller is RESET.
Bit 4	Printer Strobe	This used to indicate valid data on the printer outputs. It should be set HIGH when valid data has been written to the printer port and LOW after about 5 seconds.
Bit [5:6]		Not used.
AUX [1:2]		Not used.
Bit 7	HS3	Not used.

Interrupts

The I/O system generates two independent interrupt requests, IRQ and FIQ. Interrupt requests can be caused by events internal to IOC or by external events on the interrupt or control port input pins.

The interrupts are controlled by four types of register, status, mask, request and clear. The status registers reflect the current state of the various interrupt sources. The mask registers determine which sources may generate an interrupt. The request registers are the logical AND of the status and mask registers and indicate which sources are generating interrupt requests to the processor. The clear register allows clearing of interrupt requests where appropriate. The mask registers are undefined after power up.

The IRQ events are split into two sets of registers, A and B. There is no priority encoding of the sources.

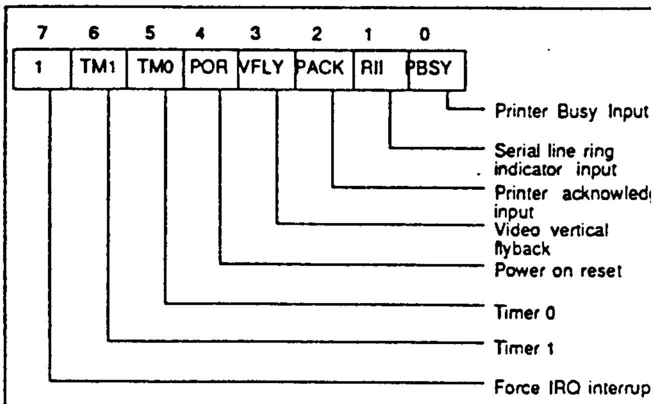
Internal Interrupt Events

- Timer interrupts TM[0:1]
- Power-on reset POR
- Keyboard Rx data available SRx
- Keyboard Tx data register empty STx
- Force interrupts 1

External Interrupt Events

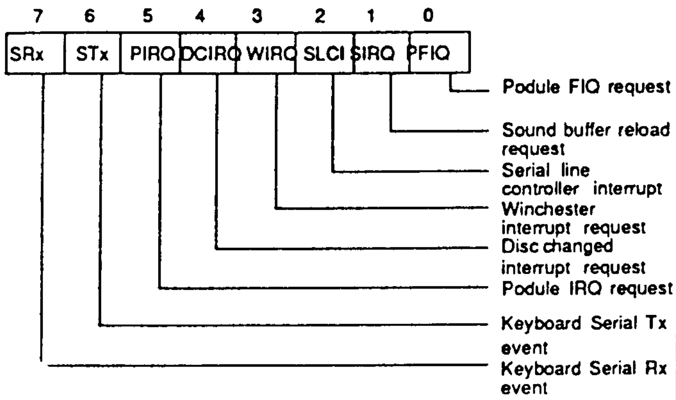
- IRQ active low inputs IL[0:7] wired as PFIQ, SIRQ, WIRQ, DCIRQ, PIRQ, PBSY and RII.
- IRQ falling-edge input IF wired as PACK
- IRQ rising-edge input IR wired as VFLY
- FIQ active high inputs FII[0:1] wired as FFDQ and FFIQ
- FIQ active low input FL wired as EFIQ
- Control port inputs C[3:5]

IRQ Status A



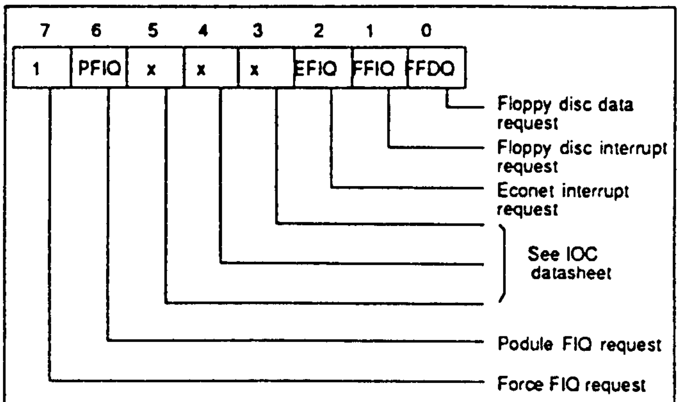
Bit	Name	Function
0	PBSY	This bit indicates that the printer is busy.
1	RII	This bit indicates that a Ringing Indication has been detected by the serial line interface.
2	Printer Ack	This bit indicates that a printer acknowledgement bit has been received.
3	Vert Flyback	This bit indicates that a vertical flyback has commenced.
4	Power-on reset	This bit indicates that a power-on reset has occurred.
[5:6]	Timer 0 and Timer 1 events	These bits indicate that events have occurred. Note: latched interrupt.
7	Force	This bit is used to force an IRQ request. It is usually owned by the FIQ owner and is used to downgrade FIQ requests into IRQs.

IRQ status B



Bit	Name	Function
0	Podule FIQ req	This bit indicates that a Podule FIQ request has been received. It should usually be masked OFF.
1	Snd buffr swap	This bit indicates that the MEMC sound buffer pointer has been relocated.
2	Serial line ctrlr	This bit indicates that 65C51 serial line controller interrupt has occurred.
3	H disc interrupt	This bit indicates that a hard disc interrupt has occurred.
4	Disc changed Interrupt	This bit indicates that the floppy disc has been removed.
5	Pod. interr req	This bit indicates that a Podule IRQ request has occurred.
6	Keyb Tx event	This bit indicates that the keyboard transmit register is empty and may be reloaded.
7	Keybd Rx event	This bit indicates that the keyboard reception register is full and may be read.

Interrupt status FIQ

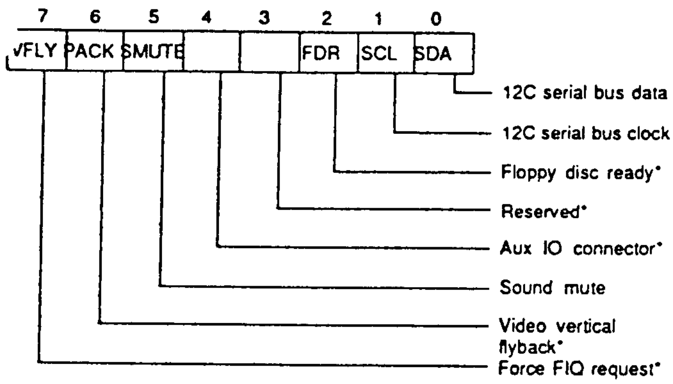


Bit	Name	Function
0	Floppy disc data request	This bit indicates that a Floppy Disc Data Request has occurred.
1	Floppy disc interrupt request	This bit indicates that a Floppy Disc Interrupt Request has occurred.
2	Econet Interrupt request	This bit indicates that an Econet Interrupt Request has occurred.
3-5,C3-5		See IOC data sheet for details.
6	Podule FIQ req	This bit indicates that a Podule FIQ Request has occurred.
7	Force	This bit allows an FIQ interrupt request to be generated.

Control Port

The control register allows the external control pins C[0:5] to be read and written and the status of the PACK and VFLY inputs to be inspected. The C[0:5] bits manipulate the C[0:5] I/O port. When read, they reflect the current state of these pins. When written LOW the output pin is driven LOW. These outputs are open-drain, and if programmed HIGH the pin is undriven and may be treated as an input.

On reset all bits in the control register are set to 1.



*must be written '1'

Bit	Name	Function
C[7]	VFLYBK and Test Mode	Allows the state of the (VFLYBK) signal to be inspected. This bit will be read HIGH during vertical flyback and LOW during display. See VIDC datasheet for details. This bit MUST be programmed HIGH to select normal operation of the chip.
C[6]	PACK & Test Mode	Allows the state of the parallel printer acknowledge input to be inspected. This bit MUST be programmed HIGH to select normal operation of the the chip.
C[5]	SMUTE	This controls the muting of the internal speaker. It is programmed HIGH to mute the speaker and LOW to enable it. The speaker is muted on reset.
C[4]		Available on the Auxiliary I/O connector.
C[3]		Reserved and should be programmed HIGH.
C[2]	READY	Used as the floppy disc (READY) input and must be programmed HIGH.
C[1:0]	SDA, SCL the IIC bus	The C[0:1] pins are used to implement the bi-directional serial I2C bus to which the Real Time Clock and battery-backed RAM are connected.

The sound system

The sound system is based on the VIDC stereo sound hardware. External analogue anti-alias filters are used which are optimised for a 20 kHz sample rate. The high quality sound output is available at a 3.5mm stereo jack socket at the rear of the machine which will directly drive personal stereo headphones or alternatively an amplifier and speakers. Two internal speakers are fitted, to provide stereo audio.

VIDC sound system hardware

VIDC contains an independent sound channel consisting of the following components: A four-word FIFO buffers sixteen 8-bit sound samples with a DMA request issued whenever the last byte is consumed from the FIFO. The sample bytes are read out at a constant sample rate programmed into the 8-bit Audio Frequency Register. This may be programmed to allow samples to be output synchronously at any integer value between 3 and 255 microsecond intervals.

The sample data bytes are treated as sine plus seven-bit logarithmic magnitude and after exponential digital to analogue conversion, de-glitching and sign-bit steering, are output as a current at one of the audio output pins to be integrated and filtered externally.

VIDC also contains a bank of eight stereo image position registers each of 3 bits. These 8 registers are sequenced through at the sample rate with the first register synchronised to the first byte clocked out of the FIFO. Every sample time is divided into eight time slots and the three bit image value programmed for each register is used to pulse width modulate the output amplitude between the LEFT and RIGHT audio current outputs in multiples of time slot subdivisions. This allows the signal to be spatially positioned in one of seven stereo image positions.

MEMC sound system hardware

MEMC provides three internal DMA address registers to support Sound buffer output; these control the DMA operations performed following Sound DMA requests from VIDC. The registers allow the physical addresses for the START, PNTR (incremental) and END buffer pointers to a block of data in the lowest half Megabyte of physical RAM to be accessed. These operate as follows: programming a 19-bit address into the PNTR register sets the physical address from which sequential DMA reads will occur (in multiples of 4 words) and programming the END pointer sets the last physical address of the buffer. Whenever the PNTR register increments up to this END value the address programmed into the START register is automatically written into the PNTR register for the DMA to continue with a new sample buffer in memory. A Sound Buffer Interrupt (SIRQ) signal is generated when the reload operation occurs which is processed by IOC as a maskable interrupt (IRQ) source.

The Memory Controller also includes a sound channel enable/disable signal. Because this enable/disable control signal is not synchronised to the sound sampling requests will normally be disabled after the waveforms which are being synthesised have been programmed to decay to zero amplitude; the last value loaded into the Audio data latch in the VIDC will be output to each of the Stereo image positions at the current Audio Sample rate.

IOC sound system hardware

IOC provides a programmed output control signal which is used to turn the internal speaker on or off, as well as an interrupt enable/status/reset register interface for the Sound Start Buffer reload signal generated by the Memory Controller.

The internal speakers may be muted by the control line SMUTE which is driven from the IOC output C5. On reset this signal will be taken high and the internal speakers will be muted.

The stereo output to the headphone socket is not muted by SMUTE and will always reflect the current output of the DAC channels.

The keyboard and mouse

The Keyboard and mouse connection to the ARM is via a keyboard controller and a serial link to the IOC. The ARM reads and writes to the KART registers in the IOC. The protocol is essentially half duplex, so in normal operation the keyboard controller will not send a second byte until it has received an ACK. The only exception to this is during the reset protocol used to synchronise the handshaking, where each side is expecting specific responses from the other, and will not respond further until it has those.

In addition to this simple handshaking system, the keyboard controller will not send mouse data unless specifically allowed to, as indicated by Ack Mouse, which allows the transmission of one set of accumulated mouse coordinate changes, or the next move made by the mouse. While it is not allowed to send mouse changes the keyboard controller will buffer mouse changes.

A similar handshake exists on key changes, transmitted as key up and key down, and enabled by Ack Scan. At the end of a keyboard packet (two bytes) the operating system will perform an Ack Scan as there is no protocol for re-enabling later. Mouse data may be requested later by means of Request Mouse Position (RQMP).

Key codes

The keyboard controller identifies each key by its row and column address in the keyboard matrix. Row and column codes are appended to the key up or down prefix to form the complete key code.

e.g. Q key down, the complete row code is 11000010 (C2 hex) and the column code is 11000111 (C7 hex).

Note: Eight keys have N key roll over. The operating system is responsible for implementing two-key roll-over, therefore the keyboard controller transmits all key changes (when enabled). The keyboard controller does not operate any auto-repeat; only one down code is sent, at the start of the key down period.

Data protocol

Data transmissions from the keyboard are either one or two bytes in length. Each byte sent by the keyboard controller is individually acknowledged. The keyboard controller will not transmit a byte until the previous byte has been acknowledged, unless it is the HRST code indicating that a power on or user reset occurred or that a protocol error occurred; see below.

Reset protocol

The keyboard controller restarts when it receives a HardReSeT (HRST) code from the ARM. To initiate a restart the keyboard controller sends a HRST code to the ARM, which will then send back HRST to command a restart.

The keyboard controller sends HRST to the ARM if :

- A power-on reset occurs
- A user reset occurs
- A protocol error is detected

After sending HRST, the keyboard controller waits for a HRST code. Any non HRST code received causes the keyboard controller to resend HRST. The pseudo program below illustrates the reset sequence or

```
START reset
ON error Send HRST code to ARM then wait for code from ARM.
IF code = HRST THEN  restart  ELSE  error
ON restart    clear mouse position counters
            set mouse mode to data only in response to an RMPS request.
            stop key matrix scanning and set key flags to up
            send HRST code to ARM
Wait for next code
IF code = RAK1 THEN send RAK1 to ARM    ELSE   error
Wait for next code
IF code = RAK2 THEN send RAK2 to ARM    ELSE   error
Wait for next code
IF code = SMAK THEN mouse mode to send if not zero and enable key scan
ELSE  IF code = SACK THEN enable key scanning
ELSE  IF code = MACK THEN set mouse mode to send when not zero
ELSE  IF code = NACK THEN  do nothing  ELSE  error
END reset
```

Reset sequencing

Direction	Code	Expected reply	Action on wrong reply (Sender)	Action on timeout (Sender)	Action if unexpected (Receiver)
ARM -> kb	Hard reset	Hard reset	Resend	Resend	Hard reset
Kb -> ARM	Hard reset	Reset Ack 1	Resend	Nothing	Hard reset
ARM -> Kb	Reset Ack 1	Reset Ack 1	Hard reset	Hard reset	Hard reset
Kb -> ARM	Reset Ack 1	Reset Ack 2	Nothing	Nothing	Hard reset
ARM -> Kb	Reset Ack 2	Reset Ack 2	Hard reset	Hard reset	Hard reset

protocol:

Note, the on/off state of the LEDs does not change across a reset event, hence the LED state is not defined at power on. The ARM is always responsible for selecting the LED status. After the reset sequence, Key scanning will only be enabled if a scan enable acknowledged (SACK or SMAK) was received from the ARM.

Data transmission

When enabled for scanning, the keyboard controller informs the ARM of any new key down or new key up by sending a two byte code incorporating the key row and column addresses. The first byte gives the row and is acknowledged by a byte acknowledge (BACK) code from the ARM. If BACK was not the acknowledge code then the error process (ON error) is entered. If the BACK code was received the keyboard controller sends the column information and waits for an acknowledge. If either a NACK, SACK, MACK or SMAK acknowledge code is received, the keyboard controller continues by processing the ACK type and selecting the mouse and scan modes implied. If the character received as the second byte acknowledge was not one of NACK/MACK/SACK/SMAK then the error process is entered.

Mouse data

Mouse data is sent by the keyboard controller if requested by a RQMP request from the ARM or if a SMAK or MACK have enabled transmission of non-zero values. Two bytes are used for mouse position data. Byte one encodes the accumulated movement along the X axis while byte two gives Y axis movement.

Both X and Y counts must be transferred to temporary registers when data transmission is triggered, so that accumulation of further mouse movement can occur. The X and Y counters are cleared upon each transfer to the transmit holding registers. Therefore, the count values are relative to the last values sent. The ARM acknowledges the first byte (Xcount) with a BACK. code and the second byte (Ycount) with any of NACK/MACK/SACK/SMAK. A protocol failure causes the keyboard controller to enter the error process (ON error).

When transmission of non-zero mouse data is enabled, the keyboard controller gives Key data transmission priority over mouse data except when the mouse counter over/underflows.

Acknowledge codes

There are seven acknowledge codes which may be sent by the ARM. RAK1 and RAK2 are used during the reset sequence. BACK is the acknowledge to the first byte of a two byte keyboard data set. The four remaining types, NACK/MACK/SACK and SMAK, acknowledge the final byte of a data set. NACK disables key scanning and therefore key up/down data transmission as well as setting the mouse mode to send data only on RQMP request. SACK enables key scanning and key data transmission but disables unsolicited mouse data. MACK disables key scanning and keydata transmission and enables the

Code values

Mnemonic	msb	lsb	Comments
HRST	1111	1111	One byte command, keyboard reset
RAK1	1111	1110	One byte response in reset protocol
RAK2	1111	1101	One byte response in reset protocol
RQPD	0100	xxxx	One byte From ARM, encodes four bits of data
PDAT	1110	xxxx	One byte from keyboard, echoes four data bits of RQPD
RQID	0010	0000	One byte ARM request for keyboard ID
KBID	10xx	xxxx	One byte from keyboard encoding keyboard ID
KDDA	1100	xxxx	New key down data. Encoded Row (1st byte) and column (2nd byte) numbers
KUDA	1101	xxxx	Encoded Row (1st byte) and column (2nd byte) numbers for a new key up
RQMP	0010	0010	One byte ARM request for mouse data
MDAT	0xxx	xxxx	Encoded mouse count, X (byte1) then Y (byte2). Only from ARM to keyboard
BACK	0011	1111	Ack for first keyboard data byte pair
NACK	0011	0000	Last data byte ack, selects scan/mouse mode. see 1.5.7
SACK	0011	0001	Last data byte ack, see 1.5.7
MACK	0011	0010	Last data byte ack, see 1.5.7
SMAK	0011	0011	Last data byte ack, see 1.5.7
LEDS	0000	0xxx	bit flag to turn LED(s) on/off
PRST	0010	0001	From ARM, one byte command, does nothing

x is a data bit in the Code; e.g. xxxx is a four bit data field

transmission of mouse count values if either X or Y counts are non-zero. SMAK enables key scanning and both key and mouse data transmission. It combines the enable function of SACK and MACK.

While key scanning is suspended (after NACK or MACK) any new key depression is ignored and will not result in a key down transmission unless the key remains down after scanning resumes following a SACK or SMAK. Similarly a key release is ignored while scanning is off.

Commands may be received at any time. Therefore, commands can be interleaved with acknowledge replies from the ARM, eg keyboard sends KDDA (1st byte), keyboard receives command, keyboard receives BACK, keyboard sends KDDA (2nd byte), keyboard receives command, keyboard receives SMACK. If the HRST command is received the keyboard immediately enters the restart sequence, see (ONrestart). The LEDS and PRST commands may be acted on immediately. Commands which require a response are held pending until the current data protocol is complete. Repeated commands only require a single response from the keyboard.

ARM commands

Mnemonic	Function
HRST	Reset keyboard
LEDS	Turns key cap LEDs on/off. A three bit field indicates which state the LEDs should be in. Logic 1 is ON, logic 0 (zero) OFF. D0 controls CAPS LOCK D1 controls NUM LOCK D2 controls SCROLL LOCK
RQM	Request mouse position (X,Y counts)
RQID	Request keyboard identification code. The computer is manufactured with a 6 bit code to identify the keyboard type to the ARM. Upon receipt of RQID the keyboard controller transmits KBID to the ARM
PRST	Reserved for future use, the keyboard controller ignores this command
RQPD	For future use. The keyboard controller will encode the four data bits into the PDAT code data field and then send PDAT to the ARM.

Mouse interface

The mouse interface has three switch sense inputs and two quadrature encoded movement signals for each of the X axis and Y axis directions. Mouse key operations are debounced and then reported to the ARM using the Acorn key up / key down protocol. The mouse keys are allocated unused row an column codes within the main key matrix.

Switch 1 (left)	Row code - 7	Column code - 0
Switch 2 (middle	Row code - 7	Column code - 1
Switch 3 (right)	Row code - 7	Column code - 2

e.g. Switch 1 release would give 11010111 (D7 hex) as the complete row code, followed by 11010000 (D0 hex) for the column code.

Note: Mouse keys are disabled by NACK and MACK acknowledge codes, and are only enabled by SACK and SMAK codes, ie they behave in the same way as the keyboa keys.

The mouse is powered from the computer 5 V supply and ma consume up to 100 mA.

Movement signals

Each axis of movement is independently encoded in two quadrature signals. The two signals are labelled REFerence and DIRection (e.g. X REF and X DIR). The table below defines the absolute direction of movement. Circuitry in the keyboard decodes the quadrature signals and maintains a signed 7 bit count for each axis of mouse movement.

Initial State		Next State		
REF	DIR	REF	DIR	
1	1	1	0	Increase count by one for each change of state.
1	0	0	0	
0	0	0	1	
0	1	1	1	
1	1	0	1	Decrease count by one for each change of state.
0	1	0	0	
0	0	1	0	
1	0	1	1	

When count overflow or underflow occurs on either axis both X and Y axis counts lock and ignore further mouse moveme until the current data has been sent to the ARM.

Overflow occurs when a counter holds its maximum positive count (0111111 binary). Underflow occurs when a counter h its maximum negative count (1000000 binary).

Keyswitch mapping

keyboard diagram

Key Size	Key Name	Row code	Col. code	Notes
1	Esc	0	0	1
1	F1	0	1	2
1	F2	0	2	2
1	F3	0	3	2
1	F4	0	4	2
1	F5	0	5	2
1	F6	0	6	2
1	F7	0	7	2
1	F8	0	8	2
1	F9	0	9	2
1	F10	0	A	2
1	F11	0	B	2
1	F12	0	C	2
1	Print	0	D	1,3
1	Scroll	0	E	1
1	Break	0	F	1
1	~	1	0	
1	1	1	1	
1	2	1	2	
1	3	1	3	
1	4	1	4	
1	5	1	5	
1	6	1	6	
1	7	1	7	
1	8	1	8	
1	9	1	9	
1	0	1	A	
1	-_	1	B	
1	=+	1	C	
1	£¤	1	D	
1	Backspc	1	E	1
1	Insert	1	F	1
1	Home	2	0	1,3
1	Pgup	2	1	1
1	Numlock	2	2	1,4
1	/	2	3	1
1	*	2	4	1
1	#	2	5	1

Key Size	Key Name	Row code	Col. code	Notes
1.5	Tab	2	6	1
1	Q	2	7	
1	W	2	8	
1	E	2	9	
1	R	2	A	
1	T	2	B	
1	Y	2	C	
1	U	2	D	
1	I	2	E	
1	O	2	F	
1	P	3	0	
1	[(	3	1	
1	])	3	2	
1.5	\	3	3	
1	Delete	3	4	1
1	Copy	3	5	1
1	Pgdwn	3	6	1
1	7	3	7	
1	8	3	8	
1	9	3	9	
1	-	3	A	1
1.75	Ctrl	3	B	1,3
1	A	3	C	
1	S	3	D	
1	D	3	E	
1	F	3	F	
1	G	4	0	
1	H	4	1	
1	J	4	2	
1	K	4	3	
1	L	4	4	
1	;:	4	5	
1	.'	4	6	
2.25	return	4	7	1
1	4	4	8	
1	5	4	9	
1	6	4	A	
1	+	4	B	1

Row and column codes are in Hexadecimal.

Notes:
1 Key colour - dark grey
2 Key colour - red
3 Key position with N key roll over.
4 Green light emitting diode under key cap.

Key Size	Key Name	Row code	Col. code	Notes
2.25	shift	4	C	1,3
1	Z	4	E	
1	X	4	F	
1	C	5	0	
1	V	5	1	
1	B	5	2	
1	N	5	3	
1	M	5	4	
1	,<	5	5	
1	.>	5	6	
1	/?	5	7	
2.75	shift	5	8	1,3
1	crsrUp	5	9	1
1	1	5	A	
1	2	5	B	
1	3	5	C	
1.5	Caps	5	D	1,4
1.5	Alt	5	E	1,3
7.0	Space	5	F	
1.5	Alt	6	0	1,3
1.5	Ctrl	6	1	1,3
1	crsrLt	6	2	1
1	crsrDn	6	3	1
1	crsrRt	6	4	1
2.0	0	6	5	
1	.	6	6	
2.0	Enter	6	7	1

Row and column codes are in Hexadecimal.

Notes:
1. Key colour - dark grey
2. Key colour - red
3. Key position with N key roll over.
4. Green light emitting diode under key cap.

Floppy disc drive

The floppy disc drive used on the A3000 computer is a one-inch high drive, taking 3.5 inch floppy discs.

Performance

Capacity	1 MB (unformatted)
Track to track step rate	3msec
Seek settle time	15msec
Write to read timing	1200µsec
Power-on to drive timing	1000msec
Power supply	+5 Volts dc
Tolerance	+/– 5%
Noise bandwidth	0 - 30 MHz
Maximum power	2Watts (continuous)

Power connector

The power connector is a 4-pin, 25mm pitch type. The LED is ON when Drive Select and In Use are low or when Drive Select is low.

Pin	Signal
1	+5
2	Ground (+5 Volts)
3	Ground
4	No connection.

Interface connector

The interface connector is a 34-way 2 row, 0.1 inch pitch type, with pinouts as shown below:

Pin		Signal
0V	Signal	
1	2	Disc change O/P
3	4	In useI/P
5*	6	Drive select 3I/P
7*	8	IndexO/P
9*	10	Drive select 0I/P
11*	12	Drive select 1I/P
13	14	Drive select 2I/P
15	16	Motor ONI/P
17	18	DirectionI/P
19	20	Step/Dsc chg rstI/P
21	22	Write dataI/P
23	24	Write gateI/P
25	26	Track 0O/P
27	28	Write protectO/P
29	30	Read dataO/P
31	32	Side 1 selectI/P
33	34	ReadyO/P

*Optionally 5V

Power supply

Performance characteristics

Performance	Min	Nom	Max	Units
Input voltage (47-53 Hz)	198	220/ 240	264	Volts ac
Input voltage (57-63 Hz)	99	115	130	Volts ac
Output voltage VO1	4.9	5	5.1	Volts dc
Output current IO1	0.5	-	4.4	Amps dc
Output ripple and noise VO1				50mV pk-pk BW 0-50MHz
Overshoot VO1				0.1Volts dc
Over voltage prot VO1 (thrshld)	5.8	-	7.0	Volts dc
Surge output current IO1	-	-	5.8	Amps dc
Surge output current duration	-	-	1.0	Sec
Efficiency	65	-	-	%@max ld
Total output power	-	-	22	Watts cont 29 Watts srge

Input voltage is selected by means of a link wire connected either to the pin marked '240' on the left-hand side of the power supply (when facing the front of the computer), or to the pin marked '120' in the top centre of the PSU.

Output socket

Pin	Signal
1	+5V
2	0V
3	N.C.
4	N.C.

Links

Link	Fitted	Effect	Default
LK22	Yes	Connection point for left channel audio speaker. P1 0V, P2 signal	None
LK23	Yes	Connection point for right channel audio speaker. P1 0V, P2 signal	None
LK5	No	Connection point for an external battery. (only used if supply of on board NiCad becomes a problem)	None
LK20	Yes	Used in conjunction with LK19 to select size of ROM devices.	Shunt 2-3
LK19	Yes	Used in conjunction with LK20 to select size of ROM devices. ROM LK19 LK20 512K 2-3 2-3 1M 2-3 2-3 2M 1-2 2-3 4M 1-2 1-2	Shunt 2-3 ie 1M
LK25	Yes	Used to configure P5 of SK14 (RGB Video Socket) to be either 'VSync' or 'Mode'. Fit shunt for 'VSync' NF shunt for 'Mode' (Mode is required by some SCART TVs)	Shunt NF ie 'Mode'
LK24	Yes	Used to configure P4 of SK14 (RGB Video Socket) to be either 'HSync' or 'CSync'. Shunt , 1-2 for 'HSync' Shunt , 2-3 for 'CSync'	Shunt 2-3 ie 'CSync'
LK27	Yes	Used to invert 'VSync' Shunt fitted , VSync* Shunt NF, VSync	Shunt NF ie 'VSync'
LK26	Yes	Used to invert 'HSync' Shunt fitted , HSync* Shunt NF, HSync	Shunt NF ie 'HSync'
LK7	No	Test point for Non Volatile Memory clock frequency. P1 0V P2 32.768KHz	None
LK30	No	Used in conjunction with LK29 and LK28 to provide the necessary signals for a Genlock interface circuit. P1 VS* P2 HS*	NF
LK28	No	P1 Ckvidc P2 Clksys*	Trk 1-2
LK29	No	P1 0V P2 Sink	Trk 1-2
LK6	No	Test point for Non Volatile Memory battery voltage. P1 0V P2 1.2V +- 0.2V	None

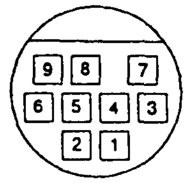
Link	Fitted	Effect	Default
LK8 LK9 LK10 LK11 LK12 LK13	No No No No No No	Used to set nationality I.D. of the keyboard.	LK12 Trk ie U.K
LK1 LK2	No No	Used to optionally link 0V to the RFI Shield (Earth)	NF NF
LK3	No	Connection point for a design backup, self contained keyboard. P1 Krst* Keyboard Reset P2 NC P3 0V P4 5V P5 Krx* From keyboard P6 Ktx* To keyboard	NF
LK4	No	Connection point for design backup, mouse to keyboard link. P1 Xr X ref P5 Sw(1) Switch 1 P2 Xd X dir P6 Sw(2) Switch 2 P3 Yr Yref P7 Sw(3) Switch 3 P4 Yd Ydir P8 0V	NF
LK17	No	Used in conjunction with LK18 to select ROM device type.	Trk 1-2
LK18	No	Used in conjunction with LK17 to select ROM device type. ROM LK17 LK18 512K EPROM 1-2 1-2 Non JEDEC 1M ROM 1-2 1-2 Non JEDEC 1M EPROM 1-2 1-2 JEDEC 1/2/4M ROM/EPROM 1-1 2-2	Trk 1-2 ie Non JEDEC
LK16	No	Used to select the design backup keyboard. See LK3. 1-2 Selects backup keyboard 2-3 Selects main keyboard	Trk 2-3 ie Main K/B
LK21	No	Selects the +5V power feed to the floppy disc drive to be via the data cable or by separate feed. 1-2 +5V via data cable 2-3 +5V via separate cable	Trk 2-3 ie not via data cable
LK14 LK15	No No	Used in conjunction with LK15 to select the keyboard uC device type. Device Type LK14 LK15 8051 (NMOS) 1-2 1-2 80C51 (CMOS) O/C 2-3	Trk 1-2 Trk 1-2 ie NMOS

Key	NF - Not Fitted P1 - Pin 1 O/C - Open Circuit Trk - Tracked * Active low

Plugs

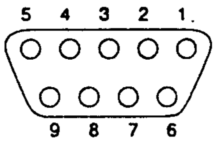
Plug	Fitted	Function/Specification
PL5	No	Floppy Disc Power Connector. If the power to the disc drive is to be supplied via the data cable, then PL5 must be fitted and the PSU free disc power socket must be connected to this plug. P1 NC P2 0V P3 0V P4 +5V
PL6	No	Floppy Disc Drive Data Connector. 34 way Box Header containing all the signals required by the internal floppy disc drive. This interface is identical to that of the Archimedes, except that the drive strength of some of the signals has been reduced as only one drive is supported. The pin numbering has been altered due to the incorrect orientation of the Archimedes layout. Default powering is via a separate power connector from the PSU (ie not up the data cable). Pin Signal — Pin Signal 2 Dcirq* — 20 Step* 4 In use* — 22 Writedata* 6 Sel(3)* — 24 Writegate* 8 Index* — 26 Track00* 10 Sel(0)* — 28 Writeprot* 12 Sel(1)* — 30 Readdata* 14 Sel(2)* — 32 Side1* 16 Motoron* — 34 Ready* 18 Dirin* 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33 all 0V
PL1	Yes	Faston tab for connection of Earth from the power supply.
PL3	Yes	Faston tab for connection of 0V from the power supply.
PL4	Yes	Faston tab for connection of +5V from the power supply.
PL2	Yes	Serial Port. (IBM PC-AT Pinout) 9 Way D-type plug. Although the plug is fitted, the interface electronics are an upgrade consisting of: IC 7 LT1133 IC 1 65C51 Pin Signal — Pin Signal 1 Dcd — 6 Dsr 2 Rxd — 7 Rts 3 Txd — 8 Cts 4 Dtr — 9 Ri 5 0V

Sockets

No.	Fitted	Function/Specification
SK1	Yes	Mouse Port. 9 way MiniDin socket providing interface to a standard Acorn (Archimedes style) mouse.  Pin Signal 1 Xr X direction reference 2 Sw(1) Switch 1 3 Sw(2) Switch 2 4 0V 0V 5 Xd X direction 6 +5V +5V 7 Yr Y direction reference 8 Sw(3) Switch 3 9 Yd Y direction
SK4	Yes	Econet Upgrade Module Socket. 17 way header used in conjunction with SK5 to provide the electrical connection point for the internal Econet upgrade module. This module is identical to that used in the BBC Master series and Archimedes computers.
SK16	Yes	Ram Upgrade Connector. A 60 way SIL pin row, providing all the necessary signals for the Acorn 1MByte Ram upgrade card.
SK3 SK11 SK8 SK9	Yes Yes No No	Internal Expansion. These connectors jointly form the internal expansion facility and are in the form of two17 way headers for SK3 & 11 and two 5 way (NF) headers for SK8 & 9. SK3 & SK11 form an 8-bit 'simple' podule bus SK3, 11, 8 & 9 form an 8-bit MEMC podule bus. A full specification of this expansion interface is provided in the chapter headed "A3000 Expansion".
SK6 SK7	Yes Yes	Keyboard Interface. Two 20 way 'flexible PCB' connectors providing an interface to the keyboard.

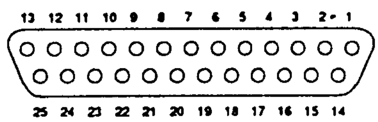
<table>
<tr><th>No.</th><th>Fitted</th><th>Function/Specification</th></tr>
<tr><td>SK14</td><td>Yes</td><td>RGB Video Socket.
9 way D type socket providing an interface to analogue RGB monitors and Scart TVs. Links 24, 25, 26 & 27 can be used to alter the polarity and type of synchronisation signals present to suit a variety of monitors.

RGB Video levels , 0.7V Pk-Pk into 75 Ohm Sync Voltage levels , >= 2.0V (TTL)



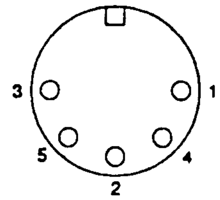
Pin Signal (IBM PC PGA pinning)
1 Red
2 Green
3 Blue
4 H/Csync
5 Vsync/Mode
6,7,8,9 0V</td></tr>
<tr><td>SK13</td><td>Yes</td><td>Monochrome Video Output.
Phono socket providing a monochrome composite video signal of 1V Pk-Pk (0.7V video, 0.3V Sync) into a 75 Ohm load. Negative sync, positive video.</td></tr>
<tr><td>SK12</td><td>Yes</td><td>Stereo Headphone Output.
3 way 3.5mm stereo jack socket providing output to personal stereo type 32 Ohm stereo headphones.

Output voltage = 1V Pk-Pk into 32 Ohm load.</td></tr>
<tr><td>SK15</td><td>Yes</td><td>External Podule Expansion.
64 Way DIN41612 socket providing an interface connection to a single, host powered, external Podule. This Podule may be a "MemC" or "Simple" type but not a Co-processor. For a full spec of this interface see the chapter headed "A3000 expansion"</td></tr>
<tr><td>SK10</td><td>Yes</td><td>Parallel Printer Port.
25 way D-type socket providing a parallel printer interface.



Pin Signal / Pin Signal / Pin Signal
1 Stb* / 8 Pd(6) / 15 nc
2 Pd(0) / 9 Pd(7) / 16 nc
3 Pd(1) / 10 Ack* / 17/25 0V
4 Pd(2) / 11 Bsy
5 Pd(3) / 12 nc
6 Pd(4) / 13 nc
7 Pd(5) / 14 nc</td></tr>
</table>

<table>
<tr><th>No.</th><th>Fitted</th><th>Function/Specification</th></tr>
<tr><td>SK2</td><td>Yes</td><td>Econet Socket.
5 way Din socket for connection to Econet local area network. Note, this interface is an upgrade.



Pin Signal
1 Data
2 0V
3 Clock*
4 Data*
5 Clock</td></tr>
<tr><td>SK5</td><td>Yes</td><td>Econet Upgrade Module Socket.
5 way header used in conjunction with SK4 to provide electrical connections for the Econet upgrade module. This module is identical to that used on BBC Master series and Archimedes computers.</td></tr>
</table>

A3000 Expansion

Internal expansion

> DANGER
>
> DANGEROUS VOLTAGES ARE EXPOSED INSIDE THE CASE OF THE COMPUTER WHEN THE COVER IS REMOVED. THE COMPUTER SHOULD BE DISCONNECTED FROM THE MAINS SUPPLY BEFORE THE COVER IS REMOVED.

The following internal upgrades are currently available for the A3000 computer:

- User port / MIDI internal expansion card
- 1 Mb Ram upgrade
- Serial port
- Econet module

Interface

The electrical signals available on the internal expansion are a subset of those described in 'A Series Podules', available from Acorn Customer Service on the SID system (Doc Ref 0310101) or as an Application Note.

The connection is via two 17-way 0.1 inch pitch connectors. Expansion cards should use 0.025 in square pin headers.

The interface is configured as 'Podule 1, Module 1'.

Expansion bus connectors

Pin no.	SK3	SK11*
1	+5v	0v
2	PWE*	+5v
3	PS1*	PRE*
4	CLK2	PRnW
5	LA[2]	LA[4]
6	LA[3]	LA[5]
7	BD[0]	LA[6]
8	BD[1]	LA[7]
9	BD[2]	0v
10	BD[3]	LA[8]
11	BD[4]	LA[9]
12	BD[5]	LA[10]
13	BD[6]	LA[11]
14	BD[7]	LA[12]
15	RST*	LA[13]
16	0v	PIRQ*
17	+5v	0v

Note: Pin 1 is at the right hand end when viewed from the front of the computer.

Power supply

The maximum power available from the +5V rail is 600 mA. The maximum dissipation inside the case is 0.5W (100mA).

5-way connectors

There is also provision on the main circuit board for two 5-way 0.1 inch connectors (these are not fitted as standard).

Pin no.	SK8	SK9
1	C[0]	0v
2	C[1]	REF8M
3	BI*	PFIQ*
4	IORQ*	Ms[1]*
5	IOGTr*	+5

Note: Pin 1 is the right hand end, when viewed from the front of the computer.

It is recommended that the load on each signal does not exceed 3HCT gates or that stated in 'A Series Podules'. Any upgrade must be able to drive at least 7 HCT and 3 TTL loads on the data bus.

Mechanical

The rear panel required is shown in the drawing at the back of this manual. The size of the User Port / MIDI expansion card PCB and position of the connectors is also shown in the drawing included at the back of the manual.

User port / MIDI expansion card (UPM)

Introduction

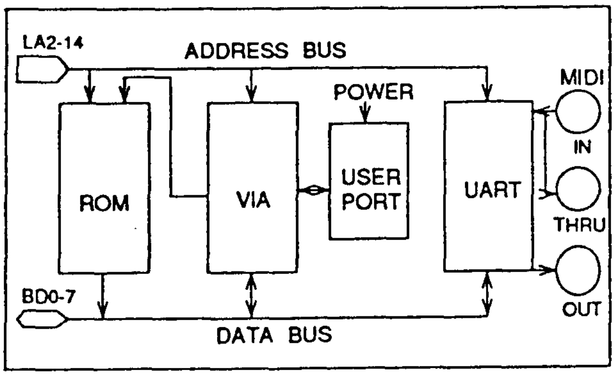
The A3000 User Port / MIDI expansion card fits inside the computer, and provides:

- An 8-bit User port, largely compatible with the User Port interface on the BBC Model B and Master 128 computers (and with the User Port on the Archimedes I/O expansion card) .
- MIDI (Musical Instrument Digital Interface), with IN, OUT and THRU connections, compatible with the International MIDI Association specification.

Main components

- 65C22 VIA for the User Port
- 2691 UART for the MIDI
- 27128 EPROM containing firmware and ID byte

Block diagram



Comparison with Archimedes expansion cards

ARCHIMEDES I/O EXPANSION CARD

The VIA is at the same address and clocked at the same speed. Port A PA<0..2> is used to page ROM. These are the same as the UPM when set for 2764/27128.

The User port is the same (Port B). The VIA interrupts go through a link, which is not normally fitted.

The MIDI section is not the same.

The ADC and 1 MHz bus are not fitted to the UPM.

MIDI EXPANSION CARD

The UART is the same (Signetics 2691), but is at a different address (see below).

The ROM page latch is not the same.

	LA13	LA12	offset address
MIDI Podule	1	0	&2000
UPM upgrade	1	1	&3000

Addresses of main system components

Address	Component
&0000-1FFC	ROM/EPROM 27128 as standard (16k x 8 bit). Larger EPROMS can be fitted if the links marked X are cut between pins 1 & 2, and relinked 2 to 3.

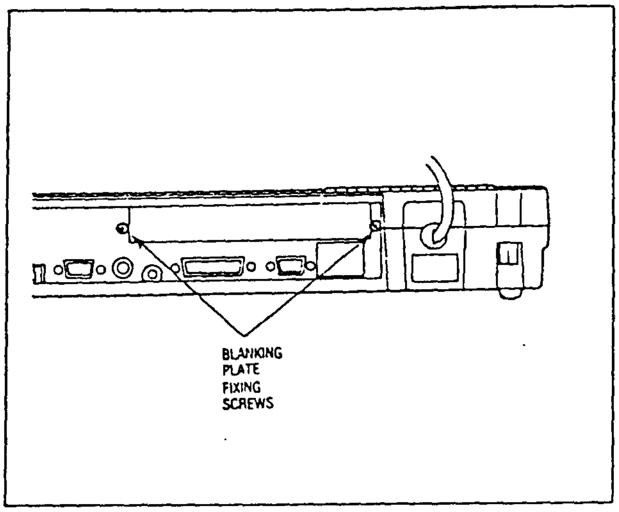
Eprom size	LK1	LK2	LK3	LK4
2764				
27128				
27256			X	
27512	X		X	
1M bit (JEDEC)	X		X	
2M bit	X	X	X	
4M bit	X	X	X	X

Address	Component
	Contains the ID byte 63 (dec).
	The start-up information must be at the top of the ROM.
&2000-2FFC	VIA 65C22 - 2Mhz part.
	Port A PA<7..0> used to page the ROM. CAs Not Used.
	Port B PB<7..0>, CB1 and CB2 for the User Port.
	Use 2Mhz synchronous cycle to access the VIA.
	The interrupt output connects directly to PIRQ*.
	No User Port interrupt handler provided.
&3000-3FFC	UART 2691 - For the Midi interface.

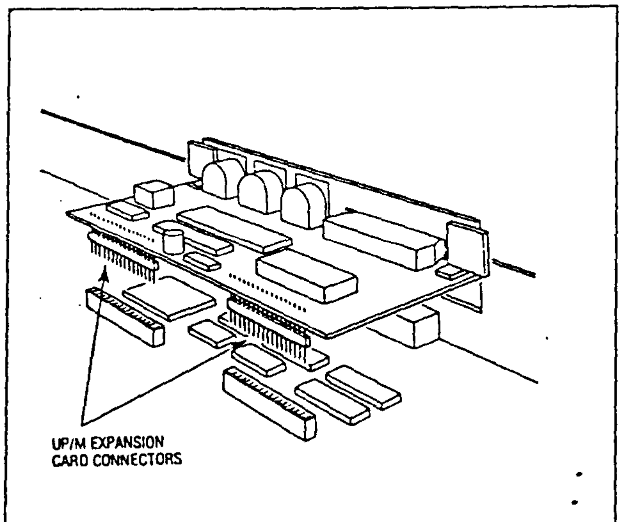
Fitting an internal expansion card

This procedure covers the fitting of an internal expansion card, such as the User Port / MIDI expansion card. This work should only be carried by Acorn Dealers or Approved Service Centres:

1 Follow the procedure for removing the cover of the computer given in the next chapter.
2 Unscrew the two machine screws holding the rear blanking plate in place:



3 Plug the expansion card into the two connectors on the PCB:



4 Replace the two screws holding the expansion card backplate.
5 Replace the cover of the computer.
6 Run the dealer test software to test the correct function of the computer and the upgrade, and of any other upgrades fitted.

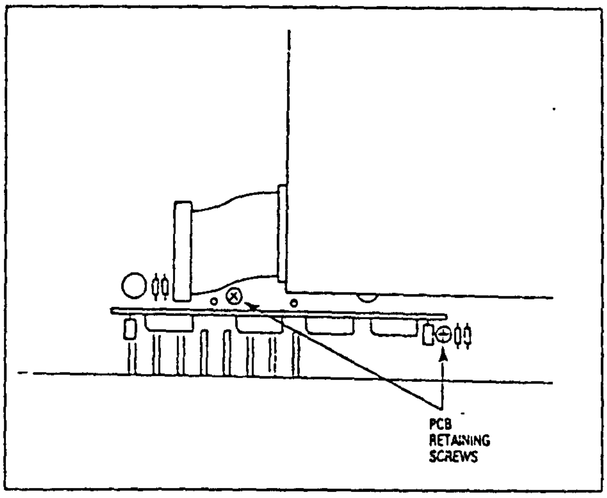
Keep the rear panel blanking plate with the computer, in case the expansion card is removed later.

1Mb RAM upgrade

The A3000 computer RAM can be upgraded from 1Mb to 2 Mb by the addition of a 1Mb RAM module which plugs into the main PCB.

Fitting a RAM upgrade

1 Follow the procedures detailed in the next chapter for the removal of the computer cover and the keyboard.
2 Remove two PCB retaining screws and plug the upgrade module, in a vertical position, into the board:



3 Replace the screws securing the PCB and the upgrade module.
4 Replace the keyboard and the cover of the computer.
5 Run the dealer test software to test the correct function of the computer and the upgrade, and of any other upgrades fitted.

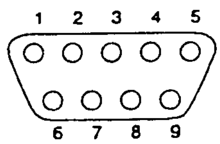
Serial port upgrade

Introduction

The A3000 computer is fitted with a 9-way D-type serial connector on the back panel, but this is not functional until a serial port upgrade kit has been fitted by an Acorn Dealer or Approved Service Centre. Only Acorn Serial Port Upgrade kits should be used.

The A3000 serial port upgrade consists of a serial processor chip and a line driver chip, which fit into existing sockets on the PCB.

Connector pinouts



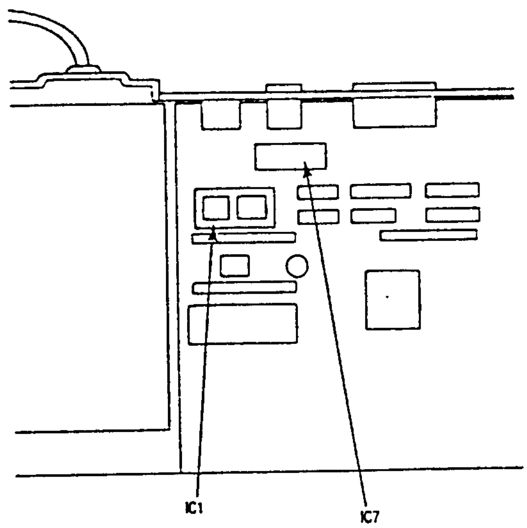
Pin	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	0V
6	OSR
7	RTS
8	CTS
9	RI

Fitting the Acorn A3000 serial port upgrade

1 Follow the procedures in the next chapter for the removal of the cover and the keyboard.

2 Remove the Econet module and the User Port / MIDI expansion card, if fitted.

3 Insert the 28-pin IC 65C51 into socket IC1, and the 24-pin IC LT1133 into socket IC7. The notched ends of the ICs should face towards the left hand side of the PCB (viewed from the front of the computer) :



4 Fit the serial number label to the PCB near the upgrade ICs.

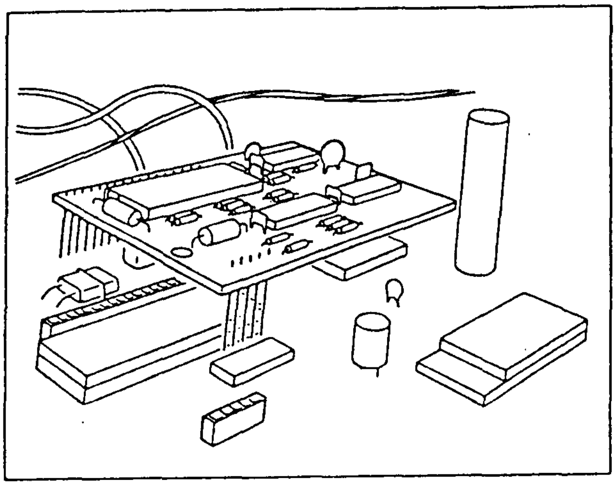
5 Refit any modules and expansion cards removed in step 2 above, and replace the cover of the computer.

6 Remove the label 'Serial not fitted' from the rear panel.

7 Run the dealer test software to test the correct function of the computer and the serial port, and of any other upgrades disturbed during this installation.

Fitting an Econet module

1. Follow the procedure for removing the cover of the computer.
2. Plug the module onto the PCB connectors:



3. Replace the cover of the computer.
4. Run the dealer test software to test the correct function of the computer and the Econet module, and of any other upgrades fitted. Refer to the appropriate Econet file server Manager's Guide for instructions on setting the station id.

External expansion

Interface

Introduction

The A3000 computer supports an external expansion card (podule) interface, although with some minor differences from other ARM based systems:

- Single +5Volt power supply rail, rated at a maximum of 1 Amp (no +12 or -5 Volt rails provided)
- No support for Co-Processor type cards
- The external expansion card is in software slot 0
- The podule must be capable of driving 3 TTL and 7HCT loads on the data bus.

Refer to the application note 'A series podules' (referenced at the start of this chapter) for a full podule interface specification.

Physical dimensions

As the podule is external to the computer enclosure there is no real limit on the size of the unit. Care should be taken not to block off any of the other expansion ports on the rear of the computer.

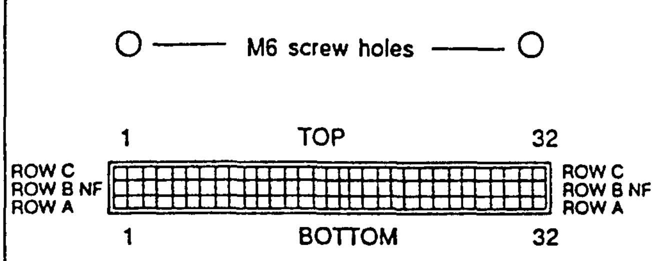
Fitting an expansion card

> WARNING
>
> Power down the computer before fitting an external expansion card.

It is anticipated that expansion cards will be fitted into an external expansion card unit. Slots are provided underneath the case of the computer, into which a tongue in the case of the expansion card unit can locate. Tapped holes are provided in the backplate of the computer to enable the expansion unit to be secured to the computer with two M6 screws.

Connector

The podule interface is provided via a 64 way DIN 41612 socket fitted at the rear of the computer:



(Connector viewed from the back of the computer)

The connections to the interface are shown overleaf.

External expansion connections

Pin	a	c	Description
1	0V	0V	Ground
2	LA[15]	reserved	
3	LA[14]	0V	Ground
4	LA[13]	0V	Ground
5	LA[12]	reserved	
6	LA[11]	$\overline{\text{MS[0]}}$	MEMC Podule select
7	LA[10]	reserved	
8	LA[9]	reserved	
9	LA[8]	reserved	
10	LA[7]	reserved	
11	LA[6]	reserved	
12	LA[5]	$\overline{\text{RST}}$	Reset (see note below)
13	LA[4]	PR/$\overline{\text{W}}$	Read/not write
14	LA[3]	$\overline{\text{PWE}}$	Write strobe
15	LA[2]	$\overline{\text{PRE}}$	Read strobe
16	BD[15]	$\overline{\text{PIRQ}}$	Normal interrupt
17	BD[14]	$\overline{\text{PFIQ}}$	Fast interrupt
18	BD[13]	$\overline{\text{S[6]}}$	
19	BD[12]	C1	I^2C serial bus clock
20	BD[11]	C0	I^2C serial bus data
21	BD[10]	$\overline{\text{S[7]}}$	External Podule select
22	BD[9]	$\overline{\text{PS[0]}}$	Simple Podule select
23	BD[8]	$\overline{\text{IOGT}}$	MEMC Podule handshake
24	BD[7]	$\overline{\text{IORQ}}$	MEMC Podule request
25	BD[6]	$\overline{\text{BL}}$	I/O data latch control
26	BD[5]	0V	Supply
27	BD[4]	CLK2	2MHz Synchronous clock
28	BD[3]	CLK8	8MHz Synchronous clock
29	BD[2]	REF8M	8MHz Reference clock
30	BD[1]	+5V	Supply
31	BD[0]	reserved	
32	+5V	reserved	Supply

Note: The $\overline{\text{RST}}$ signal is the system reset signal, driven by IOC on power-up or by the keyboard reset switch. It is an open-collector signal, and expansion cards *may* drive it also if this is desirable. The pulse width should be at least 50ms.

Disassembly and reassembly

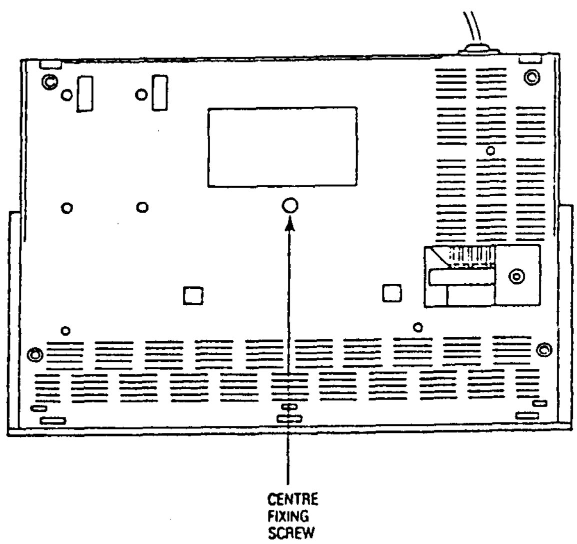
DANGER

DANGEROUS VOLTAGES ARE EXPOSED INSIDE THE CASE OF THE COMPUTER WHEN THE COVER IS REMOVED. THE COMPUTER SHOULD BE DISCONNECTED FROM THE MAINS SUPPLY BEFORE THE COVER IS REMOVED.

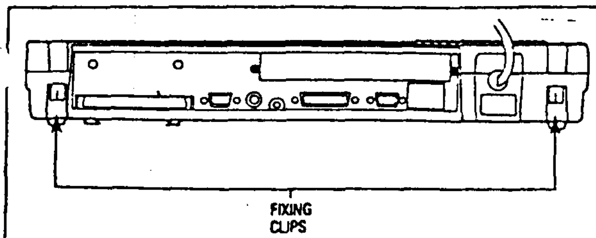
Removing the cover

To remove the cover from the computer, follow this procedure:

1 Disconnect all peripherals and unplug the computer from the mains supply
2 Unplug the mouse connector from the underside of the computer.
3 Remove the centre fixing screw on the underside of the case:



4 Remove the two screws from the clips at the rear of the computer.
5 Unhook the two clips and lift up the back of the cover, pivoting on the front until the cover lifts clear:



Fitting is the reverse of the above procedure.

Removing the keyboard

1 Follow the procedure for removing the cover.
2 Unplug the keyboard connector, and lift the keyboard out from the lower case.

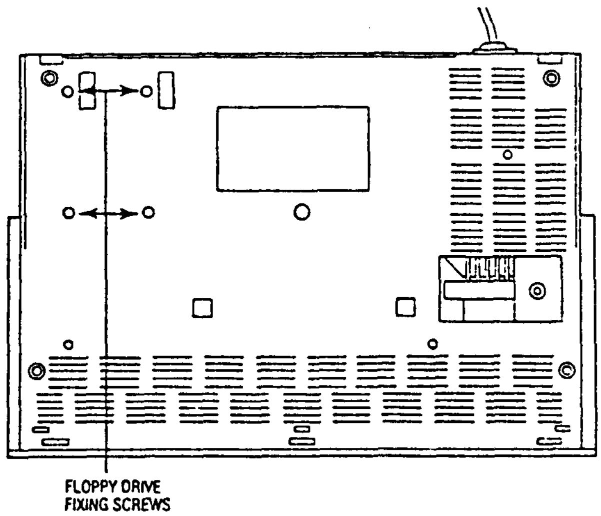
WARNING

The keyboard connector can be damaged by incorrect handling. Hold it by the white plastic strengthening strip only. Do not touch the track faces or apply pressure to the cable itself.

Fitting is the reverse of the above procedure.

Removing the floppy disc drive

1 Follow the procedure for removing the cover.
2 Disconnect the power supply cable from the drive, and the ribbon cable from the PCB.
3 Remove the keyboard (see above).
4 Turn the lower case upside down and support the drive on a foam pad.
5 Remove the four drive fixing screws:



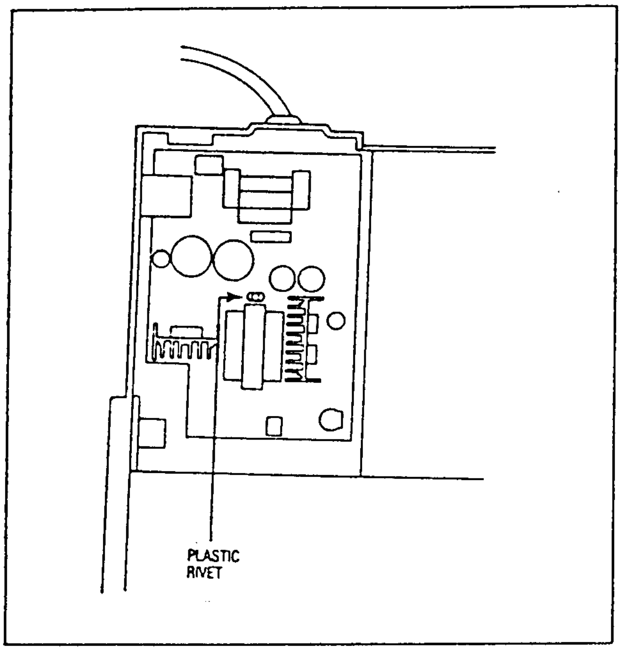
6 Support the drive and turn the case back up again. Lift the drive clear.

Fitting is the reverse of the above procedure.

Removing the PSU

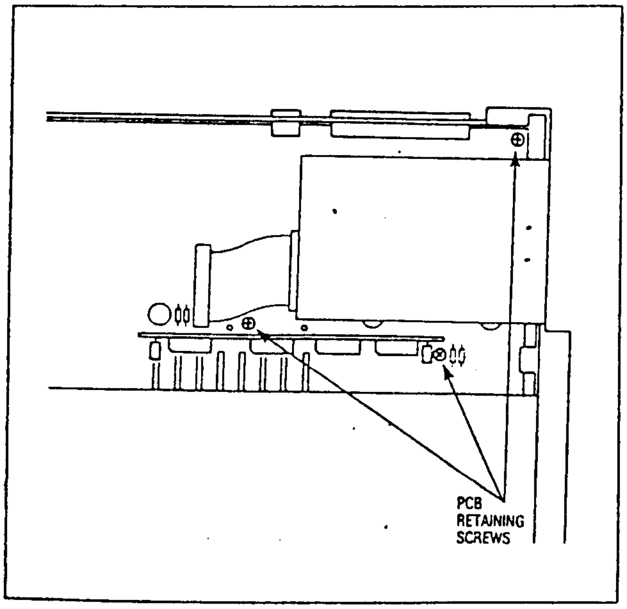
1 Follow the procedures for removing the cover and the keyboard (above).
2 Disconnect the three faston connectors from the PCB, and the cable to the disc drive.

3 Remove the warning sticker on top of the PSU cover. Push out the plastic rivet located in the centre of the PCB. The PSU and its cover will then lift out:



Removing the PCB

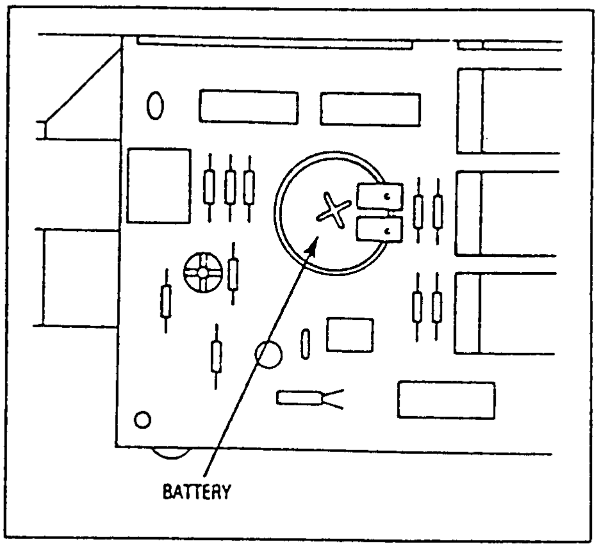
1 Follow the procedures above for the removal of the cover, the keyboard and the floppy disc drive.
2 Remove the power leads, where they connect to the PSU.
3 Disconnect the two speaker leads, and remove the RH speaker (viewed from the front).
4 Unscrew the three self-tapping screws retaining the PCB, and the PCB and rear panel will lift out of the case.



Fitting is the reverse of the above procedure.

Replacing the battery

The battery providing current to the real-time clock and battery-backed RAM is soldered to the PCB:



If this needs replacing, it will have to be removed using a soldering iron and a desoldering gun. Dealers lacking the equipment and experience in this type of work should not attempt to carry it out, or damage to the PCB may result.

Fault diagnosis

Introduction

This chapter is a guide to the diagnosis and repair of basic faults in the A3000 computer system.

It consists of alforithms to enable you to trace & remedy faults in a 'dead' computer, followed by instructions for running the functional test software, designed to isolate faults in acomputer which is working.

The next chapter 'Main PCB fault diagnosis and repair' is designed to help those repair centres equipped to do so, to diagnose and repair faults at component level on the main PCB.

Test equipment required:

- 100 MHz oscilloscope
- DC Voltmeter
- Earth Continuity tester
- Serial port loopback plug
- 32 ohm impedance headphones
- Chip extraction tools
- Antistatic matting and wrist straps
- standard hand tools

DANGER

WHEN REFITTING OR FITTING A REPLACEMENT ASSEMBLY, CHECKS SHOULD BE MADE FOR EARTH CONTINUITY BETWEEN THE EARTH PIN OF THE MAINS PLUG AND THE FOLLOWING:

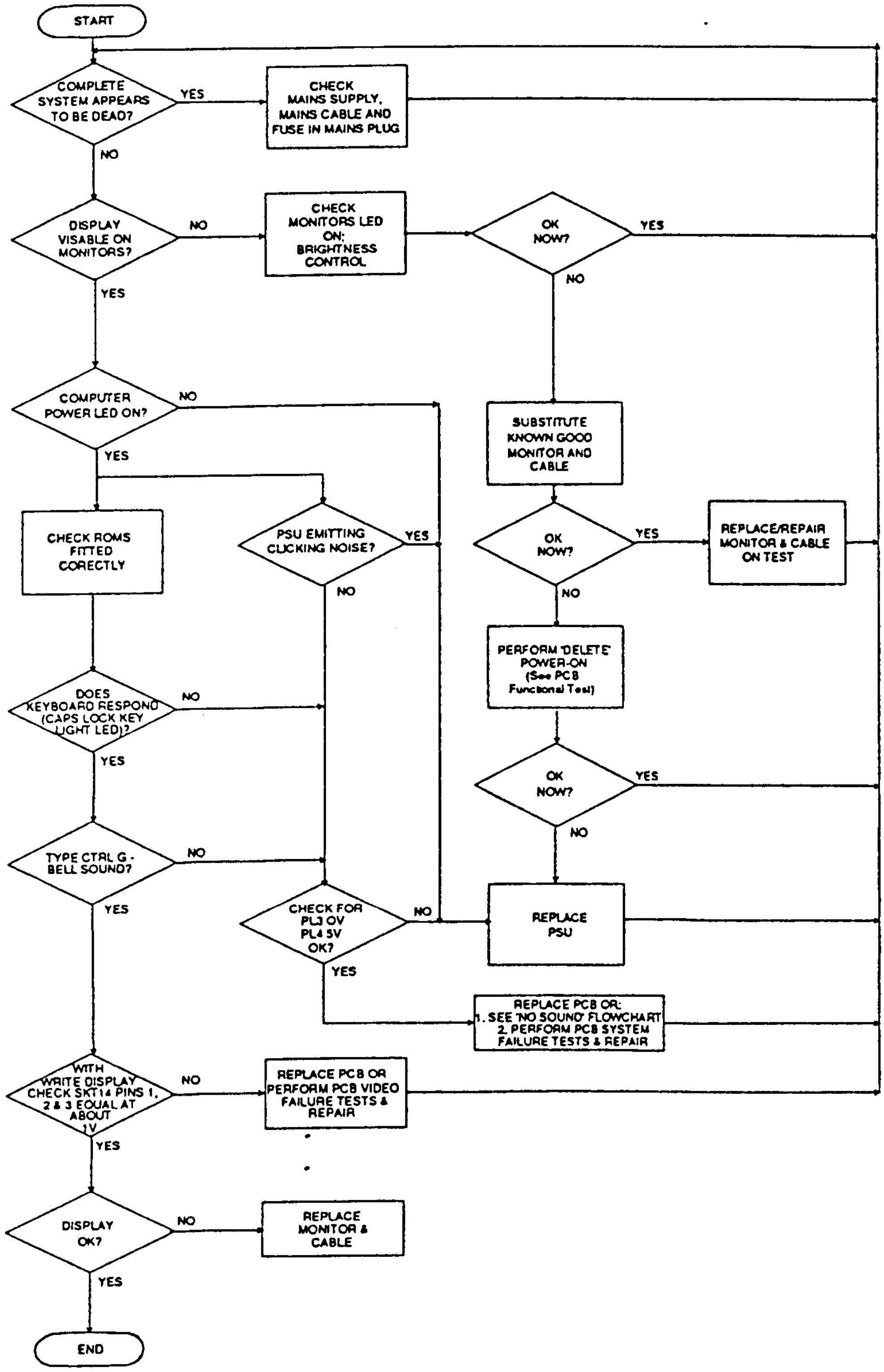
- THE REAR PANEL INTERNAL EXPANSION CARD FIXING SCREWS
- BOTH PRINTER/PARALLEL PORT D TYPE FIXING BOLTS
- THE TOP COVER

USE AN EARTH CONTINUITY TESTER SET TO 25 AMPS.

WARNINGS

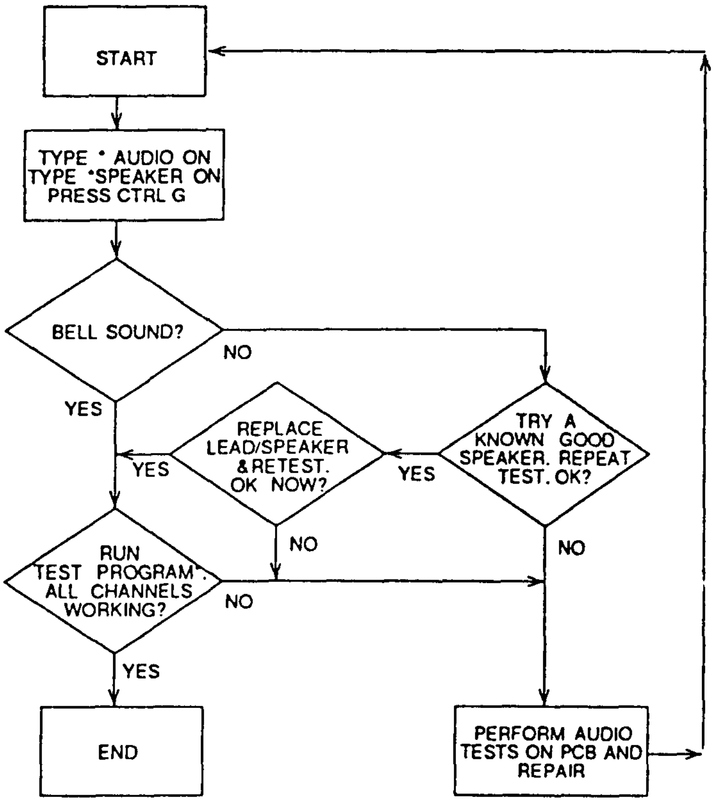
- Repairs to multi-layered PCBs:
  The main PCB is a four-layer board. Components should only be removed from the board using equipment specifically designed for this purpose. For details of suitable equipment available, contact Acorn Customer Service.
- Repairs to surface-mounted devices:
  The ARM, MEMC, IOC AND VIDC ICs on the A3000 PCB are surface-mounted components. Do not attempt to remove them from the board and replace them unless you have the correct equipment to do so.
- System clock failure:
  If the computer is powered on for more than a few seconds and there is no system clock, there is a risk that all four ARM chips may be damaged, as well as the RAM.
- Faulty MEMC:
  If MEMC is faulty or the RAS/CAS signals are not being generated, the RAM may be damaged if the machine is left on too long. If you suspect a fault in these areas, scope the RAS and CAS lines for a few seconds in order to make sure that they still active, then turn the machine off. Do not leave the computer on for more than a few seconds at a time.

Checking a 'dead' computer



Checking the sound system for faults

Note: Both SoundDMA and SoundChannel modules must be active (ie, not unplugged) before starting this test.



*TEST PROGRAM

```
10 REM > Check all channels
20 VOICES 8
30 FOR channel-1 TO 8
40 OSCLI("Channelvoice "+STRS(channel)+" "+STRS(2))
50 NEXT
60 FOR channel - 1 to 8
70 SOUND channel, -15, 100,24
80 PRINTchannel
90 k-GET
100 NEXT
```

RUN PROGRAM.
PRESS A KEY AND REPEAT EIGHT TIMES.
PRINTS CHANNEL NUMBER TO THE SCREEN
AND PLAYS VOICE 2 FOR EACH CHANNEL.

Functional tests

Notes:
- Please read the following section 'General test procedure' before you carry out any of the tests.
- For details of how to repair the main PCB, see Main PCB fault diagnosis and repair.

Introduction

The A3000 test disc (part number 0282,032) enables the engineer to test the functionality of the computer and Acorn upgrades, and to isolate any faults which may appear. The functional test cannot of course be run on a 'dead' computer - see the previous section for advice on diagnosing faults in 'dead' computers.

General test procedure

The A3000 computer, mouse, backplane, expansion cards, Test disc, Port Tester assembly and Econet cables are designed and specified by Acorn Computers Ltd and may not be changed without written consent from Acorn. All items should be complete with the correct cables so that you can connect them to the A3000 computer.

Equipment required

- A3000 computer to be tested
- Mouse
- 3.5 inch Test disc, part number 0282,032
- Two ADFS 800k formatted, write enabled, 3.5 inch discs, to be labelled Scratch Disc and Data disc.
- Serial port 'loopback' plug for A3000
- Epson FX80 or Olivetti JP101 printer
- Pair of 32 ohm stereo headphones
- Mono monitor
- Analogue RGB monitor.

Note: You can replace the specified printers with any other manufacturer's direct functional equivalent (in terms of BOTH hardware interface and software).

Connecting up the equipment

Connect the:
- serial port 'loopback' plug to the 'SERIAL' socket
- printer to the 'PARALLEL PRINTER' port
- headphones to the 'Headphones 32 ohm' socket
- monochrome monitor to the 'MONO VIDEO' socket
- analogue RGB monitor to the 'ANALOGUE RGB' socket
- monitors to the mains supply
- A3000 computer to the mains supply.

Removing the top cover of the computer main unit

Remove the top cover of the A3000 computer as detailed in the previous chapter 'Disassembly and Assembly'.

Connecting and disconnecting the power

- You must CONNECT the power only when you have made all the other connections
- You must DISCONNECT the power before removing any other connections.

It is important to disconnect the equipment from the computer in the correct order, ie disconnect the:
1. computer from the mains supply
2. monitor from the mains supply
3. mono monitor
4. analogue RGB monitor
5. headphones
6. printer
7. serial port 'loopback' plug
8. mouse.

Validating the test equipment

Before carrying out any of the tests in this section, validate the test equipment using a known good system. If the test equipment fails, you should repair the test equipment and retest on a known good part.

Before you start

Before the start of each day or testing session, you must first:
- Adjust the colour monitor to ensure adequate contrast and brightness
- Inspect all the mechanical parts of the test equipment and replace any parts as necessary.

Also, if required:
- Ensure that the printer has sufficient paper
- Connect the printer and monitor to the mains supply. Do NOT turn on.

Saving the CMOS RAM

The tests alter the contents of the battery backed RAM that holds the A3000's configuration data. These must be saved before any of the tests are run, and restored when the last test is over.
1. Insert the Test disc into the floppy disc drive (Part no. 0282,032).
2. Switch on the computer.
3. If your screen is showing the desktop environment, use the mouse to click on the 'EXIT' icon, otherwise, type *GOS.
4. At the RISC-OS supervisor prompt (an asterisk) type the following;

```
DRIVE 0
```

CMOSLS

5 When prompted, replace the Test disc with an ADFS 800k write enabled disc, the data disc.
6 Type 'S' to save the contents of the RAM, or 'L' to load a previously saved copy of the RAM.
7 Type the filename to use.
8 When prompted, replace the Test disc in the drive and press the space bar to continue.
9 Put the data disc in a safe place. Do NOT use this disc for the later floppy disc test.
10 Type 'Q' to quit this option.

Powering on

Before beginning the test, ensure that you have saved the CMOS RAM. Then:

1 Turn on all equipment EXCEPT the computer.
2 Insert the test disc into the floppy disc drive.
3 Whilst holding down the 'Delete' key, turn the computer on. If the 'Delete' power-up is successful, a red border appears momentarily on the screen before the Desktop environment appears.
4 If the display is not stable, switch off the computer and repeat the procedure described in step 3.

Carrying out the tests

There are two types of tests - subjective and non subjective. The test program passes or fails the equipment on the non-subjective tests; however, you must judge whether the equipment passes or fails the subjective tests. It is a good idea for testers to familiarise themselves with the correct results given by a known good computer. In this way they will be in a better position to judge faulty results.

Performing soak tests

At the successful completion of a main PCB functional test, you should carry out a soak test. To do this, select the relevant option and then insert the scratch disc when prompted. The test runs for 12 hours. When the test is running the Caps Lock and Num Lock LEDs will flash, provided that no error has occurred. If a disc error occurs all the LEDs will be off (see table below); the disc error is also displayed on the screen. If the test is completed without an error then the Scroll Lock LED will flash and the Caps Lock and Num Lock LEDs will be extinguished.

	Num Lock	Caps Lock	Scroll Lock	Result
No errors	Flashing	Flashing	Off	Running
Error	Off	Off	Off	Fail
Finished	Off	Off	Off	Pass

Warning

During the soak test the unit under test should not be subjected to mechanical shock or movement. The unit shall not be turned off unless the test has terminated – the pass or fail message will be displayed.

Safety check

After repairing a unit, and after the soak test, you should carry out the earth continuity check mentioned at the start of the chapter, followed by a further run-through of the functional test, in case the earth check causes malfunction in the computer.

Repairing faults

When repairing an A3000 computer, you should repair the faults in the order in which they occurred during the test (ie repair the first recorded failure FIRST).

For further information on checking for faults and carrying out repairs, refer to the appropriate section of this manual.

Restoring the CMOS RAM

After passing the soak test, the unit under test needs to be restored to the customer's configuration. This is carried out by reloading the CMOS RAM from the data disc saved earlier, by selecting the Load/Save CMOS RAM option from the main menu. Then select the Load option after inserting the Data disc when prompted. See 'Saving the CMOS RAM' above for details of the test procedure.

Packing

After servicing, repack the A3000 computer in its box. To avoid damage, do NOT send the computer through the post or by courier unless it is in its original packaging.

Main functional test

Running the test

Run the main functional test software as follows:

Ensure that CMOS RAM contents have been saved to disc by using the Load/Save CMOS RAM option on the start-up menu. Then restart the system with a delete-power-on. To perform a delete-power-on, do the following: Whilst holding down the <Delete> key, turn the unit, under test, on. Note that the <Delete> key needs to be held down for several seconds. The screen should display the DESKTOP environment.

Note: A useful indication of the success of the delete-power-on sequence is the momentary appearance of a red border area on the screen.

Insert the Test disc. Hold down Shift and * and press Break.

The 'Dealer Test Menu' is displayed:

```
A3000 Dealer Test Menu
1  Main Computer
2  Upgrades
3  Load/Save CMOS RAM
4  Soak Test
5  Quit
SELECT OPTION :
```

Select the option `Main computer.`

After selecting and loading the required test program, the A3000 computer cycles through a series of tests beginning with the computer type/model test. This test is extremely fast and the type and model number of the computer is displayed immediately:

```
This computer is a
BBC A3000

CHECK DESCRIPTION
THEN PRESS <SPACE> TO CONTINUE
```

You should:

1 Check that the description displayed on the screen is correct.

2 If `Unknown UUT` is displayed then one of the following is incorrect. Check the following:

a) MEMC is performing calculations too slowly.
b) Memory fault.

ACTION: Change the main PCB, or see the next chapter for repair.

3 If an RS232 or 1Mb RAM upgrade is fitted but not mentioned, switch off the unit under test, remove the upgrade and then continue the test. When the computer has passed the main test sequence, power down the unit and install the upgrade and then run the relevant upgrade test.

4 If the description is the same, press the space bar to the next test.

Test Options

```
TEST OPTIONS

A All Tests Except Printer
B All Tests and Epson Printer
C All Tests and JP101 Printer

SELECT OPTION
```

Select the test for the printer connected to the A3000. If you do not want to test the printer and do not need a print out of the results, you can select the 'All Tests Except Printer' option.

Memory

The Functional test continues by testing the memory. The screen clears and displays the following messages:

```
Memory test
-----------

Phase one: incrementing pattern ....

Phase two: TRUE hierarchy .............
.......

Phase three: FALSE hierarchy ..........
..........

Phase four: Cycling bits ..............
..................

PASSED/FAILED message

Press SPACE to continue.
```

A failed message will end the tests.

ACTION: Change the main PCB, or see the next chapter for repair information.

If the test has PASSED, press the Space Bar to continue the test.

Battery backed RAM

The test continues by testing battery backed RAM. The following message is displayed on the screen:

```
Battery Backed Ram (BBR) test running.

Reading BBR into main memory.

Checking read/write function of BBR.

Re-loading configuration parameters.

PASSED/FAILED message

PRESS <SPACE> TO CONTINUE

Press the Space Bar to continue the test.
```

ACTION: Check battery holders and connections, and check battery is charged. Re run the test.If the test still fails, replace the main PCB, or see the next chapter for repair information.

Time

The Functional test continues by testing the time and date settings. A series of options is displayed on the screen:

```
DO YOU WANT TO ?

1. CHECK THE DATE AND TIME
2. SET THE DATE AND TIME
3. CHECK THEN SET THE DATE AND TIME

PRESS 1 OR 2 OR 3
```

The normal procedure is to select option 1. If you want to reset the time or date you would select 2 or 3. For example, you can:

1 Type 1 to check the date and time.
2 Check that the time is correct and the seconds are incrementing correctly.
3 To continue with the test, press the Space Bar.

Loudspeaker

The functional test continues by testing the operation of the loudspeaker. A short repeating sequence of four notes is played, first through the left and then the right speaker. The following message is displayed:

```
LOUDSPEAKER TEST
LISTEN AND CHECK SOUND
THEN PRESS <SPACE> TO CONTINUE
```

You should:

1 Listen to the sequence of notes.
2 Check that the first four notes come from the left speaker and the second four from the right.
3 Check that the sound produced is correct.
4 This is a subjective test, so if you detect any deviation, make a note of the fault.

Action if test fails

If no sound, or sound from one speaker only then check speaker connections. If it still fails, substitute known good speakers and re-test. If the sound is not stereo check that the headphone plug is inserted correctly. If test still fails, replace the main PCB, or see the next chapter for repair information.

To continue with the test, press the Space Bar.

Headphones

The Functional test continues by testing the 'Headphones 32 ohms' socket. The following message is displayed as the test proceeds:

```
HEADPHONE TEST RUNNING
LISTEN AND CHECK SOUND
THEN PRESS <SPACE> TO CONTINUE
```

The test consists of a repeating sequence of eight musical notes. The first four notes are played on one headphone and the next four notes on the other headphone.

1 Put on the headphones.
2 Listen to the sequence of notes.
3 This is a subjective test, so if you detect any deviation in either headphone, note down the fault.

Action if test fails

If no sound or poor/faulty sound on known good headphones, replace the main PCB, or see the next chapter for repair information. Ensure the headphones are plugged in correctly.

4 To continue with the test, press the Space Bar.

Standard colour monitor

This test consists of a series of screen displays. You proceed through the test at your own pace.

The first display consists of a series of white lines radiating from the top lefthand corner. A cursor, in the shape of a bird, travels across the screen, starting from the bottom left and finishing at the top right. The features to check are:

- the accuracy of the lines
- the movement and integrity of the cursor.

This is a subjective test, so make a note of any faults.

When you have finished looking at the screen display, press the Space Bar to move to the next display.

The next screen displays consist of four test cards. There is a test card for each of the three colour guns, and a 'grey scale' to test the three guns. The four test cards are:

- Red scale
- Green scale
- Blue scale
- Grey scale.

Each test card consists of 16 concentric circles beneath a horizontal band which is divided into 16 sections. A pale border highlights the left most eight sections of the band in order to distinguish the band from the background. The whole test card is surrounded by a contrasting border.

The purpose of the cards is to display 16 shades with the shade of the border as the middle of the range. You should observe:

- the 16 shades displayed
- the mid-coloured border
- the quality of the 'grey scale' display
- the integrity of each test card.

This is a subjective test, so make a note of any faults which you detect and when you are ready to continue press the Space Bar.

Action if test fails

If display rolls or is unstable, perform 'Delete' reset until correct default value obtained. The computer may have lost its configuration value for SYNC. Type at the keyboard:

```
*CON. SYNC 1 (RETURN)
```

press reset RESET and see if if any change occurs. If no improvement, change the main PCB.

Colours incorrect or missing

With a full white screen, VIDC IC 8 pins 39, 40 and 41 should all have the same signal on them. If not, change the main PCB.

Keyboard Functional Test

Keys stuck

During this test, any keys or mouse buttons which are in a permanently closed position (ie stuck down) are displayed on the screen. If any keys are permanently closed, then it will be impossible to continue the test.

If everything is normal and no keys are stuck then nothing is displayed on the screen and the Test program passes straight on to the next test.

LEDs

This test checks that the LEDs, Caps Lock, Scroll Lock and Num Lock are working. To carry out this test:

1 Follow the instructions which appear on the screen. These tell you when to check that each LED is ON and OFF.
2 Note down any LED failures before continuing the test.
3 After each set of instructions press Break to move to the next instruction.

Mouse

This tests the three buttons on the mouse and the movement of the mouse to the left, right, up and down. Each of the mouse buttons (ie left, middle, right) are displayed on the screen in turn, together with a pointer. You should:

1 Move the mouse, until the pointer is within the box on the screen, then press the displayed button on the screen.
2 Press the corresponding mouse button. The button displayed on the screen should disappear and the next button appear.

If the button cannot be made to disappear then it will be IMPOSSIBLE to continue the test. You should repeat the test with the known good mouse to isolate the fault to either the keyboard or the mouse. Replace faulty components, then retest.

If everything is normal, the program moves on automatically to the next test.

Keys

The screen clears to show a representation of keys in the main keyboard area. You need to test each key in turn in the correct order ie work from the bottom line of the keyboard and from left of the keyboard to the right:

1 Press Caps Lock.
2 Check that the picture of the Caps Lock key disappears from the screen.
3 Press Shift and check that the picture of the Shift key disappears from the screen. If the picture of the key does not disappear from the screen then leave a small delay before pressing the next key.

If the screen stops clearing the characters as you press the keys, go back to the lowest, left most key remaining on the screen and start again from there.

4 Continue working along the bottom line. Then, start working from left to right along the next line up.

Note: If you accidentally press two keys together, you will see both keys displayed on the screen. You should press Break to continue.

If the same fault occurs repeatedly or the picture of the depressed key refuses to disappear, then it will be IMPOSSIBLE to continue the test. You should repair the keyboard and start the whole test again.

5 When all keys in the main keyboard area have been pressed successfully the screen clears and displays a diagram of the rest of the keyboard area. Again, press each key in turn, following the guidelines above.
6 When all the keys have been successfully pressed, the screen clears and displays the following message:

```
MOUSE TEST - PASSED

MAIN KEYBOARD TEST - PASSED

NUMERIC KEYPAD TEST - PASSED

PRESS RESET BUTTON TO END TEST
```

Press the Reset button on the side of the unit. You have now finished the keyboard functional test.

Action if tests fail

Make sure that the configuration items 'DELAY' and 'REPEAT' are set to sensible values - see the User Guide.

If the keyboard PCB is replaced, re-run the keyboard functional test.

Floppy disc drive

The Floppy disc drive test consists of two parts. The first part of the test checks the write protect mechanism. The test disc must be write protected for this test to work. If the A3000 disc drive passes the following message is displayed:

```
FLOPPY DISC DRIVE TESTS
Checking write protect
PASSED/FAILED Write Protect

Insert Scratch Disc
Then press SPACE
```

Replace the Test disc with an ADFS 800k write enabled disc, the scratch disc. Any data already on this disc may be destroyed, so it is best to use a blank disc.

The test continues with disc Read, Write and Erase tests. Each test gives a PASSED/FAILED message.

Action:

If test fails, check that the configuration for 'STEP' and 'FLOPPIES' is correct. Check the disc drive ID switch is set to the correct position - normally '0' for single floppy drive, '1' for second floppy drive.

Swap the cable and drive for known good examples. Check power to to drive. If fault persists, change the main PCB.

RS 232

On selection the test will automatically run and give a PASSED or FAILED message.

Action:

If the test fails, make sure that the configuration items 'BAUD' and 'DATA' are set to sensible values. If the test still fails, after you have ensured that the loopback slot is functional on another unit, change the main PCB. If a fault is reported but the test has passed, then refer to the diagram of the loopback socket in the appendix for explanations.

Printer

If one of the printer options was set, a test pattern is sent to the printer. The pattern comprises a repeated series of stepped lines each representing bits 0 to 7. You should look for missing or corrupted pattern. As this is a subjective test so make a note of any faults that you detect.

Action:

If the test fails with a known good printer and cable connected, check the configuration settings for 'PRINTER' and 'IGNORE' are correct. If fault still persists, change the main PCB.

On completing the tests

On completing the tests the screen displays:

```
TESTS COMPLETE
```

and outputs a message to the printer. This indicates that the A3000 computer has passed all the non-subjective tests. However, the message Tests Complete should NOT necessarily be interpreted as a PASS, since you may wish to fail the computer on one of the subjective tests.

If a failure has been found during the non-subjective tests, the screen displays a FAILED message and lists the failures on the printer, assuming that the printer is functioning and that you did not select the 'All Tests Except Printers' option from the menu. Insert the Test Disc and press 'space' to return to the main menu.

Upgrade tests

Introduction

Run the relevant Upgrade tests detailed below; if it fails, substitute a known good upgrade. If the test still fails, replace the main PCB, or see the next chapter for repair information.

A3000 User Port MIDI Upgrade

Introduction

The UPM Upgrade functional test should be carried out whenever you install, repair or replace an UPM Upgrade. The suite of programmes provide assistance when fault finding, by providing a continuous looping.

Note: The MIDI 'Thru' port is NOT tested.

Equipment required

In order to carry out the test, you will require the following equipment:

- UPM Upgrade to be tested, which should have been installed
- A3000 Computer
- 3.5 inch Test Disc, write protected
- Monochrome or analogue RGB monitor.

To test the UPM Upgrade you will require the following additional equipment:

- Acorn Econet cable
- User port loopback plug
- Dual trace oscilloscope, if you are fault finding.

Connecting the equipment

Connect the:

- Computer to the monitor
- MIDI IN socket to the MIDI OUT socket, using the Econet cable
- User port loopback plug to the User port
- Monitor to the mains supply
- A3000 to the mains supply.

Running the test

After powering up the computer, you should select the relevant options from the menu, ie Upgrades, and then MIDI.

```
A3000 UPM UPGRADE DEALER TESTS

1 Functional test.

2 Functional test soak.

3 Services routines.
```

```
Enter choice
```

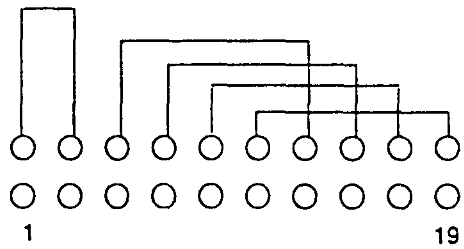
Select the appropriate test from the menu; all tests load automatically.

Selections 1 and 2 give a PASSED or FAILED message.

Selections 3 gives a further choice, after which a 'Running' message indicates that the selected routine is functioning and the associated signals can be traced with an oscilloscope.

Action if failed

Check that the test leads are working and are plugged into the correct sockets. If the test still fails then try using a known working PCB. If this passes then replace the MIDI podule under test, or else replace the main PCB.



UPM Upgrade loopback plug (20 way IDC)

1 Mbyte DRAM Expansion Test

Running the test

Select the relevant menu option for the 1MByte DRAM Expansion Test.

Action if test fails

Ensuring the CMOS RAM contents have been saved to disc by using the Load/Save CMOS RAM option on the start-up menu. Then restart the system with a delete-power-on. To perform a delete-power-on, do the following: Whilst holding down the <Delete> key, turn the unit, under test, on. Note that the <Delete> key needs to be held down for several seconds. The screen should display the DESKTOP environment.

Note: A useful indication of the success of the delete-power-on sequence is the momentary appearance of a red border area on the screen.

To restart the test hold down the <Ctrl>, <shift>, and <*> keys whilst pressing and releasing the <Break> key. Select the relevant options to run the 1 Mb memory upgrade test.

If the test still fails, check the connection between the main PCB and the memory expansion card. If test fails yet again, try a known working memory card. If this fails then replace the main PCB, else replace the faulty memory card.

RS 232

On selection the test will automatically run and give a PASSED or FAILED message.

Action

If the test fails, make sure that the configuration items 'BAUD' and 'DATA' are set to sensible values (BAUD 4 and DATA 4, for example). If the test still fails, after you have ensured that the loopback socket is functional on another unit, change the main PCB. A circuit diagram for the loopback plug is included in the Appendices.

Action resulting from test failure

The following notes refer to the test procedures on the PCB functional test disc, and the action that should be taken as the result of a test failure.

Memory:	Perform memory tests, section XX, and repair as necessary.
Battery-backed RAM:	Perform NVM and RTC tests, and repair as necessary.
Loudspeakers:	If no sound, check speaker connections. Substitute a known good speaker and re-test. If OK, replace speaker. If test still fails, perform AUDIO tests, and repair as necessary.
Headphones:	If no sound or poor/faulty sound on known good headphones, perform AUDIO tests and repair as necessary. See also Production and Field Changes.
Monitor Screen:	If display rolls or is unstable, perform R reset until correct default value obtained. If no improvement, perform Unstable or Scrolling Display tests, and repair as necessary. If the display breaks up around its edges and spurious characters appear suspect the system oscillator. See Corrupted Display. Colours incorrect or missing - With a full white screen, VIDC IC 41 pins 39, 40 and 41 should all have the same signal on them. If not, change the VIDC IC41.
Floppy Disc:	See Floppy disc drive.
Serial port:	If test fails, see 'Serial Port', in the next chapter.

Main PCB fault diagnosis & repair

System failure

If the system appears to be dead, proceed as follows:

1 Check for main system clock of 24 MHz on LK28. If absent, check again on IC47, pins 3, 4, 5 and 6, and change IC47 if required. Finally, change the crystal X3.

2 Check for clocks on IC44 pin 67 and IC41 pin 19.

3 Check that the signal RST driving IC 44 pin 44 and IC 37 pin 9 is not stuck high.

4 Check for the presence and validity of the processor addresses and PHI 1 clock. This can be done by examining the signals on IC 29 pins 12 to 19, IC 30 pins 12 to 19 and IC 31 pins 12 to 15, whilst holding down the RESET button. In this situation the processor continuously increments its address bus. Should any of the signals not toggle, suspect either a short or open circuit on that line. Should none of the signals toggle, check for the PHI 1 clock on the appropriate IC and at its source on IC 44 pin 66 and on R135. Also check to see that addresses are being presented to the inputs of the above devices. Change ICs 29, 30 or 31 as appropriate, or if no addresses are present, change the ARM IC 37.

5 The data bus can be inspected by probing on resistors R49 to R65, R115 to R128 and R87. By their nature, it is difficult to interpret the signals seen, so just check for the ability of the signals to move between logic states. None of these lines should be stuck permanently high, low or in a midrail state. Any of these resistors may be removed in order to isolate the DRAM bank from the CPU, thus easing the tracing of shorts, etc. Also check for short or open circuits on the BDATA bus, IC 43 pins 12 to 19 and IC 46 pins 12 to 19.

6 Check for shorts on DRAM address bus, either on the DRAMS themselves or on IC 44 pins 28 to 37.

7 Check for Data and Address signals on all four of the ROMs. This is especially important if a ROM change has been carried out, as misuse of a screwdriver during ROM removal may have damaged or broken PCB tracks, socket or ROM legs.

8 Check for all address lines on MEMC, IC44, again with RESET held down.

9 Check for the presence of LA2 to LA6 and LA16 to LA21 on IOC IC13.

10 Check the processor interrupt lines FIQ and IRQ pins 8 and 7 on ARM IC 37. Neither of these should be stuck low. IRQ can be expected to pulse low, FIQ should be high. These interrupts should also be checked at their source on IOC IC13 pins 50 and 51. Should these also be low, the interrupt source can be traced by examining all interrupt inputs to IOC IC 13 on pins 30 to 42 (note that pins 30, 31 and 42 are active high logic).

11 Check for a RAS signal on pin 5 of all the DRAMS.

Video faults

Video failure

1 Check for +5 V on both ends of L18. If open circuit then check C100 for a short circuit. Replace L18 and C100 as appropriate. Also check for 3.5 Volts (approx.) on IC 41 pin 43. Should this not be present then check R109, D16 and C93.

2 Check for a 24 MHz clock on IC41 pin 19. If missing then check continuity to and through LK28 and R138.

3 Check for video data on IC41 pins 39, 40 and 41. If not present, check power supply to IC41.

4 Check for short circuits on signals VIDRQ and VIDAK.

5 Check connection of all data lines to VIDC (IC41).

6 Finally, change IC41.

Unstable or scrolling display

The computer may have lost its configuration value for SYNC. Type at the keyboard:

```
*CON. SYNC 1 (RETURN)
```

Press reset RESET and see if if any change occurs. Investigate configuration failure.

Check for CSYNC signal on SK14 pin 4. If not present, trace back through LK24, R534 and IC40, finally changing VIDC IC41.

Check settings of LK24 and LK26 (see Links table).

Corrupted display

If the display breaks up around its edges and spurious characters appear then investigate the system oscillator. Suspect IC47or X3.

Check DRAM using the memory test routines.

Colours incorrect or missing

With a full white screen, VIDC IC41 pins 39, 40 and 41 should all have the same signal on them. If not, check pin 43, which should show approximately 3.5V; if not, check R109, C93 and D16. Finally, change VIDC, IC41.

Trace each signal through the periphery circuitry and out to SK14, where the voltage on R, G and B should be

the same.

Audio

Test the audio with both headphones and internal speakers. Do not forget to issue *SPEAKER ON and *VOLUME 127 commands, if required, making sure that the sound modules are active (see the 'No sound' algorithm in the previous chapter).

If either of the speakers fail, but the headphone socket functions normally, check connections to the main PCB via LK22 and LK23, and check IC32 or IC38 pin 5 for a signal of 2-3 V amplitude. If no signal is present on pin 5 but can be found on pin 3, change IC32 or 38. Check continuity through R76 and R45 and check that IC13 pin 49 is not stuck high.

If there is no audio at all, first check for +5 V on both ends of L19. If this is open circuit, check the condition of C108 before replacement. Check for about 3 V on VIDC IC41 pin 12. If there is no voltage or a different one, check R500, C107 and C108.

A low amplitude signal should be found on VIDC IC41 pins 13, 14, 15 and 16. If not, change VIDC. These signals can be traced through the peripheral circuitry and out to Q11 and Q12. The signal amplitude at these points should be about 1.3 V pk-to-pk.

Check for short or open circuit on signals SNDAK and SNDRQ on VIDC IC41 pins 9 and 24.

Configuration, NV Memory and RTC

If the NVM suffers data retention problems and the RTC fails, then, with the computer power off, check for about 1.1 V on IC6 pin 8. If this voltage is not present, check R3 and R7. If less then 1V, change the battery B1 and check the operation of D2 and C15.

If the NVM IC6 consistently fails on the same data bits, change the device.

If the clock fails to run or runs inaccurately, check and if necessary replace X2. LK7 allows access to the clock signal.

Peripheral faults

Keyboard and mouse

Make sure that the configuration items DELAY and REPEAT are set to sensible values - see the A3000 User Guide.

Check computer interface by swapping to a known good keyboard or mouse.

Floppy disc drive

Make sure that the configuration items STEP and FLOPPIES are correctly set. Check that the disc drive ID selection switch is in the zero position. Swap the disc drive for a known good drive and cable. If this also fails, check the power supply connection for +5 V and 0 V.

If the computer is not recognising the drive, check that all cables are connected both to the drive and to the PCB, and that power is present on the power cable. Also check that the drive ID plate has not fallen off inside the drive and jammed it.

Printer

Make sure that the configuration items for IGNORE and PRINT are set to sensible values. Swap the printer for a known good printer and cable.

If the printer fails completely, check for a STROBE signal on Q1 collector; trace back through R36 and IC18. Also check for shorts or open circuits on PACK and PBSY on pins 2 and 4 of IC9, and 11 and 13 of IC8.

If the data printed is incorrect, check the continuity of the data lines into and out of IC 11, though the series resistors and onto SK 10.

If both the printer and the floppy disc drive fail, change IC 18.

Capacitors C23 to C33 on the printer port occasionally go open circuit. These should be checked if printer problems are being experienced.

Serial port (upgrade)

Check that the upgrade has been correctly installed. Make sure that the configuration items BAUD and DATA are set to sensible values. Check for ≈10V on IC7 pin 1 and ≈-10V on pin 24. Check for the clock on IC 1 pins 6 and 7; change X1 if faulty. If OK, change IC1 and IC7.

Expansion cards

Run the relevant expansion card test; if it fails, substitute a known good expansion card. If the test still fails, check through System failure, tracing all signals through to the expansion card socket SK15 (external) or SK3 and 11 (internal). If necessary, replace expansion card backplane.

Test ROMs

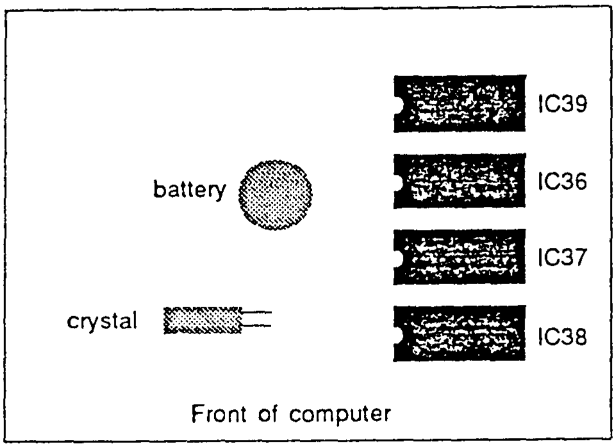
The A3000 Test ROMs are designed to assist in the repair of all A3000 systems where 'Failure to Initialise' faults are present - ie the machine appears to be 'dead' on power-up.

The ROMs contain software which can be categorised in two sections:

1 Main memory test routines

2 Test routines for use under repetitive reset.

To install the test ROMs, carefully remove the RISC OS ROM set, ICs 14, 15, 16 and 17, and replace them with the test ROMs, 1, 2, 3 and 4 respectively:



Use the bare minimum of hardware to run the system - remove/disconnect all peripherals not needed for the tests.

Main memory test

Providing that the ARM, MEMC and VIDC are functioning, the test ROMs will auto-boot into the menu-driven display below. At any point in the operation of the test ROMs, pressing the RESET key or re-powering the machine will re-start the program and re-display the menu:

```
012345678901234567890123456789012345678901234567890123456789012345

  A1 DIAGNOSTIC TEST ROMS MEMORY SIZE -&0XX00000 BYTES

 1.  CYCLIC MEMORY TEST WITH PRINTOUT

 2.  CYCLIC MEMORY TEST


  SELECT:
```

The memory test checks memory according to memory size selected.

It is possible that faulty memory may lie in the region designated as 'screen memory'. If this occurs, the video display may become unreadable. For this reason, the sequence 0123456789 is repeated across the top line of the display. Every 4 digits represents a 32-bit word. Watch for missing or corrupted display.

As the start of the screen memory is known to be at physical address &2000000, it should be possible to determine the exact device that is faulty by examining the corruption pattern on the display.

The default 'memory size' is &100000 bytes (1 Mbyte), however this may be cycled through 0.5, 1, 2 and 4 Mbyte memory sizes by pressing the 'M' key.

When using the ROMs on a machine having memory content other than 1 Mbyte, the video display may at first appear out of line or incorrect. In this instance press the M key repeatedly until the required memory size has been selected.

The memory test is cyclic and on completion of each full memory test a full stop (.) will be displayed. The 0.5 Mbyte test takes between 3 and 4 seconds to complete whilst the 4 Mbyte test takes about 29 seconds.

If for some reason the video display is completely blank or unreadable (eg because of a video fault), a printed output may be obtained by selecting option 1, the output being produced at the printer port as well as on the VDU.

If an error is found in the memory, the display will show:

```
AT ADDRESS &nnnnnnnn WROTE &pppppppp READ xxxxxxxxxx
xxxxxxxxxxxxxxxxxxxxxx
```

(The message will be displayed on one line) where nnnn is the faulty address, pppp is the data written to that address and xxxxxxxx is the data read back from that address in binary form.

The memory tests do not terminate unless an error is found, in which case after reporting 8 or 9 errors, the test will terminate.

An additional check is now made on the state of CMOS RAM control lines C0 and C1. If either of these lines are short-circuit to 0 Volts, the Test ROMs will indicate this on power-up.

Memory map	
Physical Address	IC Numbers
&2000000	IC21 IC20
&2000001	IC22 IC23
&2000002	IC24 IC25
&2000003	IC26 IC27
repeat until	
&20FFFFF	
&2100000	upgrade
to	
&21FFFFF	

Repetitive reset test

This section of test code is intended for use when the main memory test menu fails to initialise.

To make use of this section of the ROMs the following test equipment is required:

- Oscilloscope
- Signal or pulse generator

The purpose of the code is to produce certain signals around specific areas of the PCB. These signals may then be monitored using the oscilloscope to assess the operation of that area of the circuit.

The code is written in a loop which should execute three times before proceeding to the main memory test. For this reason the machine must be reset repeatedly.

A suitable square wave or, preferably, a negative-going pulse generator output at 10 kHz should be connected to the reset line via a component connected to IOC IC13 pin 29.

After setting the border colour to white, the signals should be observable in the following order:

SVPMD	low
SVPMD	low
SVPMD	low
IOC CS & S1	hi
IOC CS & S2	hi
IOC CS & S3	hi
IOC CS & S4	hi
IOC CS & S5	hi
IOC CS & S6	hi
IOC CS & S7	hi
nB/W	low
nB/W	low
nB/W	low
IOC CS & C0	hi
IOC CS & C1	hi
IOC CS & C2	hi
IOC CS & C3	hi
IOC CS & C4h	hi
IOC CS & C5	hi
IOC CS	hi

Return to start for three executions.

After execution of this code, the border colour is reset to black. The assembler listing for this section of the code is given below:

```
Start1      LDRT    r0,       [r5]          ;SVPMD pin low          )
            LDRT    r0,       [r5]          ;                       )continual toggle of:-
            LDRT    r0,       [r5]          ;                       )
            LDR     r1,       iocmof        ;re-load ioc base addr. -offset
            LDR     r0,       [r1,r6]!      ;SVPMD pin high
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S1 ioc hi
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S2 ioc hi
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S3 ioc hi
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S4 ioc hi
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S5 ioc hi
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S6 ioc hi
            LDR     r0,       [r1, r6]!     ;IOC CS pin high        ;S7 ioc hi

            LDRB    r0,       [r5]          ;nB/W pin high          )
            LDRB    r0,       [r5]          ;nB/W pin high          )
            LDRB    r0,       [r5]          ;nB/W pin high          )
            MOV     r1        #&FE0000      ;
            STR     r1,       [r7]          ;  set C0               )
            MOV     r1        #&FD0000      ;                       )
            STR     r1,       [r7]          ;  set C1               )
            MOV     r1        #&FB0000      ;                       )
            STR     r1,       [r7]          ;  set C2               )
            MOV     r1        #&F70000      ;                       ) I.O.C.
            STR     r1,       [r7]          ;  set C3               )
            MOV     r1        #&EF0000      ;                       )
            STR     r1,       [r7]          ;  set C4               )
            MOV     r1        #&DF0000      ;                       )
            STR     r1,       [r7]          ;  set C5               )
            MOV     r1        #&FF0000      ;
            STR     r1,       [r7]          ;  reset all

            LDR     r1,       &55555555     ;  write to printer port
            STR     r1,[r8]                 ;

            SUBS    r9, r9, #1
            BNE     start1

BmainM
```